MULLARD LIMITED
Mullard House
Torrington Place
London, W.C.1

CONTENTS

Monochrome tv power supplies for 117 and 220V mains inputs 26-28
Thyristor power supplies for colour tv receivers 29-34
Luminance, colour-difference output, synchronising and a.g.c. circuits 35-45
Thermostatic fan control for central heating 46-48

VOL. 11 No. 102 NOVEMBER 1969

Mullard Technical Communications

VOLUME 11 NUMBER 102

November 1969

Mullard Technical Communications

VOLUME 11 NUMBER 102 November 1969

Contents

Monochrome tv power supplies for 117 and 220V mains inputs *D. J. King* 26

Thyristor power supplies for colour tv receivers *D. J. King* 29

Luminance, colour-difference output, synchronising and a.g.c. circuits *M. C. Gander and L. Hampson* 35

Thermostatic fan control for central heating *S. W. Gray* 46

Mullard Technical Communications records new developments in the application of electronics in science, industry, and the home. It contains information on the properties and performance of discrete and integrated semiconductor devices, electronic valves and tubes, and associated magnetic, electrical, electron-optical, and electromechanical components and assemblies. The practical circuits given are, in general, designed to provide the best working conditions and most favourable performances for the devices used. Where design principles are discussed, these may be used (so far as device ratings allow) for adaptation of the published designs to meet particular requirements. Current data sheets should always be consulted before any circuit or adaptation is considered for production.

All information is published in good faith, but no guarantee of performance is given or implied. Nor does publication imply any authority or licence for the utilisation of any patented feature.

Of the devices or assemblies included in circuits, Mullard Limited can normally supply only those listed in the Company's current catalogues. Availability in large quantities should be confirmed with Mullard Limited.

Technical enquiries should be addressed to the Editor, not to the authors or laboratories.

Six issues are published each year. Circulation (free of charge) is limited to equipment designers, research organisations, laboratories, libraries, educational establishments, and engineering consultants. Requests for addition to the mailing list must be made on the official stationery of the establishment concerned.

Abstracts, or references to an article, should mention both the source, *Mullard Technical Communications,* and the authors. Requests for republication or translation should be made to the Editor in writing. All articles in *Mullard Technical Communications* are indexed in *British Technology Index*. Abstracts appear in *Current Papers in Physics, Electrotechnology, and Control.*

'Mullard' is the trade mark of Mullard Limited and is registered in most of the principal countries of the world.

Editor: F. A. Sowan Assistant Editor: E. G. Evans

Central Technical Services
Mullard Limited, Mullard House, Torrington Place, London, W.C.1
Telephone: 01-580 6633 Telex: 264341

© Mullard Limited, 1969

Made and Printed in England by
WIGHTMAN AND COMPANY LIMITED, 1/3 BRIXTON ROAD, LONDON, S.W.9

Monochrome tv power supplies for 117 and 220V mains inputs

D. J. King
Mullard Central Application Laboratory

UDC621.397.13:621.311.62[621.382.333.4]

The use of a thyristor as a controlled half-wave rectifier enables a stabilised and low impedance 145V h.t. line to be obtained from a 220V a.c. mains input. By the addition of a voltage doubling circuit at the input and a single pole changeover switch, an economic power supply, suitable for a solid state monochrome receiver, may be designed to accept a.c. mains inputs of 90 to 140V and 160 to 264V.

INTRODUCTION

In an all-transistor monochrome receiver a main h.t. line of 145V is required to supply the line deflection and video circuits. This article describes a thyristor power supply which can provide a stabilised 145V line at some 400mA and operate with a.c. mains inputs in the range 160 to 264V.

An additional circuit is described, having the same performance, which can operate with an a.c. mains input as low as 90V. This increased range of operation is achieved by switching in a voltage doubling circuit, comprising a capacitor and diode, with a single pole changeover switch.

The latter type of supply provides the facility whereby a receiver could be operated anywhere in the world when used with the appropriate tuner/i.f. circuit. Furthermore, operation on a 525-line system is possible using a transformerless vertical timebase (Ref. 1).

DESIGN POSSIBILITIES

With a half-wave diode rectifier connected directly to the 220V mains, some 300V would be produced at the reservoir capacitor. By dropping this voltage with a high value resistor, which would also provide excellent smoothing, an h.t. line of 145V could be obtained. Although this high impedance supply would produce poor e.h.t. regulation (typically 8MΩ) and the picture size would also vary with changing mains voltage, these effects would no doubt be tolerated if this was the cheapest solution, particularly for second receivers.

Extra expense would be involved, however, in obtaining the l.t. supplies for the audio, field and signal processing circuits. The use of line timebase scan rectification to obtain these supplies cheaply would introduce severe technical problems, since the spreads in l.t. voltage due to mains voltage and beam current variations would result in very high collector dissipations in the various circuits. Therefore, the more costly method of using a mains transformer and 50Hz rectifier system would be required for the l.t. supplies.

The alternative concept of a receiver using a thyristor power supply to provide a low impedance stabilised h.t. line, and deriving the l.t. supplies by scan rectification, can be very competitive when overall receiver costs are considered. By using a thyristor power supply, the e.h.t. regulation is reduced (typically to 3MΩ), the picture size remains constant and the performance of the timebase is much improved. This improvement in performance also applies to the rest of the receiver circuits whose supplies are derived from the line timebase.

With the thyristor supply, the improved receiver performance can be obtained with mains inputs in the wide range 160 to 264V.

RECEIVER POWER REQUIREMENTS

In a solid state receiver a BU105 high voltage transistor is employed in the line deflection circuit and is operated from the stabilised 145V h.t. line. The required mean current is some 200mA when the e.h.t. current to the picture tube is 300μA. This is increased to some 340mA when the receiver l.t. supplies, which normally total 20W, are obtained by scan rectification. When the h.t. currents of the line oscillator, driver and video stages are added, the total h.t. current required by the receiver is typically 400mA maximum.

CIRCUIT DESCRIPTION

To obtain a stabilised h.t. line directly from the mains, a thyristor is used as a half-wave rectifier (Ref. 2) whose conduction point is controlled to occur in the latter half of the positive half-cycle of the mains input. The conduction point of the thyristor determines the d.c. voltage, and hence control of this point enables a stabilised d.c. output to be obtained. A suitable circuit designed to meet the receiver power requirements is shown in Fig. 1. In this circuit a diac CSR$_1$ is used to apply a pulse of current to the gate of the thyristor CSR$_2$ causing it to conduct. This trigger pulse is obtained when the breakover voltage of the diac, which is developed across C$_1$, is reached.

To stabilise the output, the trigger point is varied as a function of mains input and d.c. output. Transistor TR$_2$ is used to control the charging current of C$_1$ and hence the trigger point for the thyristor. The base circuit of the transistor is connected to a potential divider across the mains input to sense input changes and vary the base current, thus controlling the charging current of C$_1$. Feedback from the d.c. output is also applied to the transistor by R$_4$ and any tendency for changes in output voltage, due for example to load current variations, is again controlled. This simple stabilisation circuit minimises the effects of mains voltage variations or load changes on the d.c. output voltage.

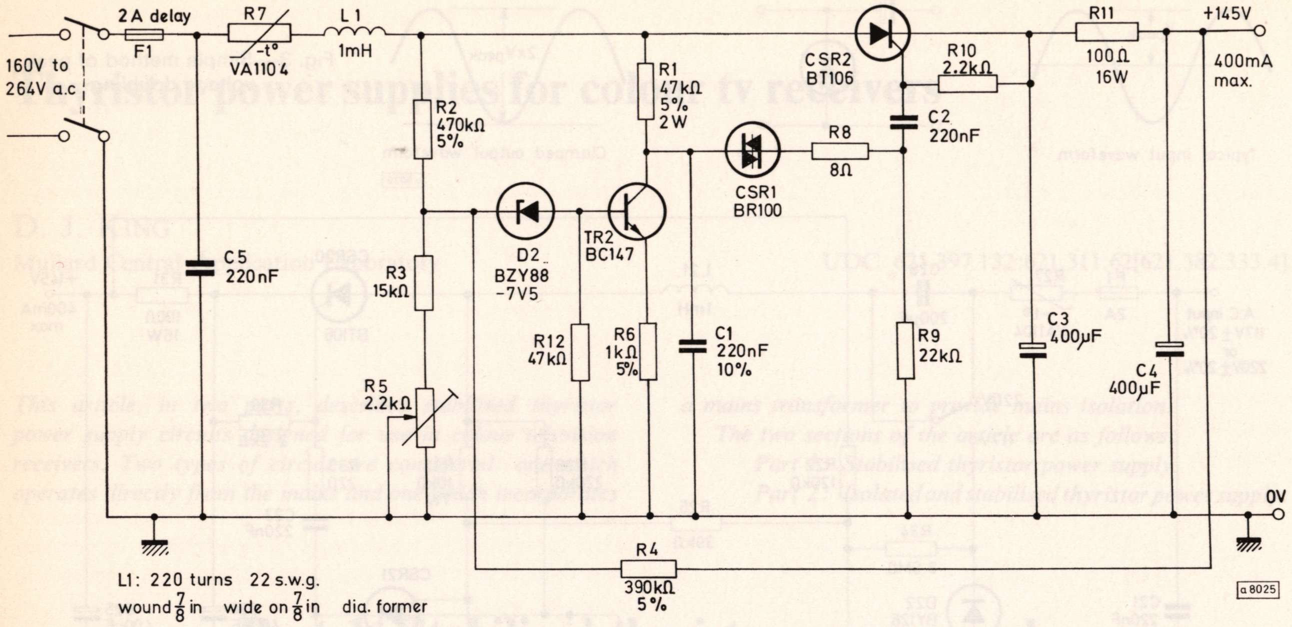

Fig. 1—Stabilised thyristor d.c. power supply

PERFORMANCE

Graphs of the power supply load characteristic and the effect of mains variations are shown in Fig. 2. The output voltage is substantially constant with mains inputs from 264V (240V+10%) to 187V (220V−15%) and only starts to fall in the region of 160V, when the thyristor is fully conducting at the peak of the mains input waveform.

At this point the circuit behaves as a normal RC smoothed diode rectifier configuration with the output voltage falling in proportion to the mains input and load current. The smoothing circuit has been designed to reduce the hum on the output to some 600mV. Raster movement with this hum level is imperceptible.

LOW MAINS CIRCUIT

Most European countries have a.c. mains supplies which are predominantly in the 200 to 250V region, but there are large areas of the world where the supplies are around 110V. Typical of these is Japan, 100V±10%, and all of the Americas where plug-in appliances must operate on 117V±10% mains. To fully meet the receiver power requirements from these mains inputs, the thyristor power supply would have to accept inputs from mains waveforms where the peak value is less than the smoothed d.c. output. It is possible, however, to increase the peak value of the mains waveform by the simple addition of the d.c. restoring circuit shown in Fig. 3. With this configuration the negative half-cycle of the mains waveform is clamped to the negative power supply rail. Thus the full peak-to-peak voltage of the input waveform is made to be positive-going and suitable for controlled rectification by the thyristor circuit. The d.c. restored input waveform has a mean d.c. value and the charge capacitor C$_1$ is no longer discharged on the negative half-cycle of mains input. For stable operation it is necessary to fully discharge this capacitor each cycle of mains input.

A diac is not designed to 'break-back' to zero after firing and, therefore, cannot discharge C$_1$ completely. A more suitable device for use with this type of input

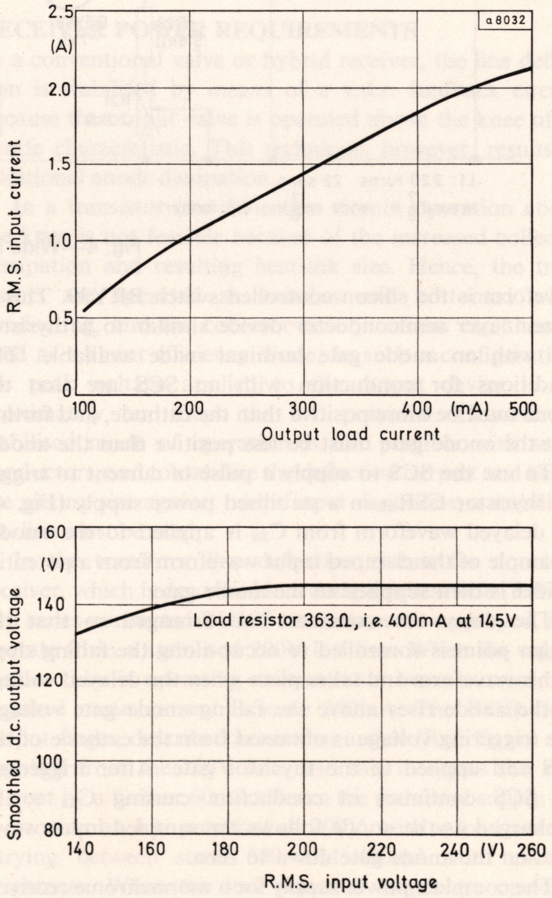

Fig. 2—Power supply characteristics

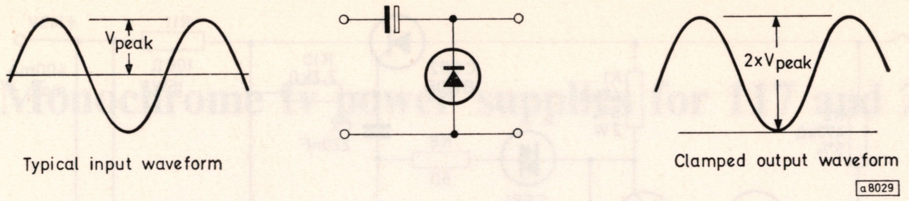

Fig. 3—Simple method of peak voltage doubling

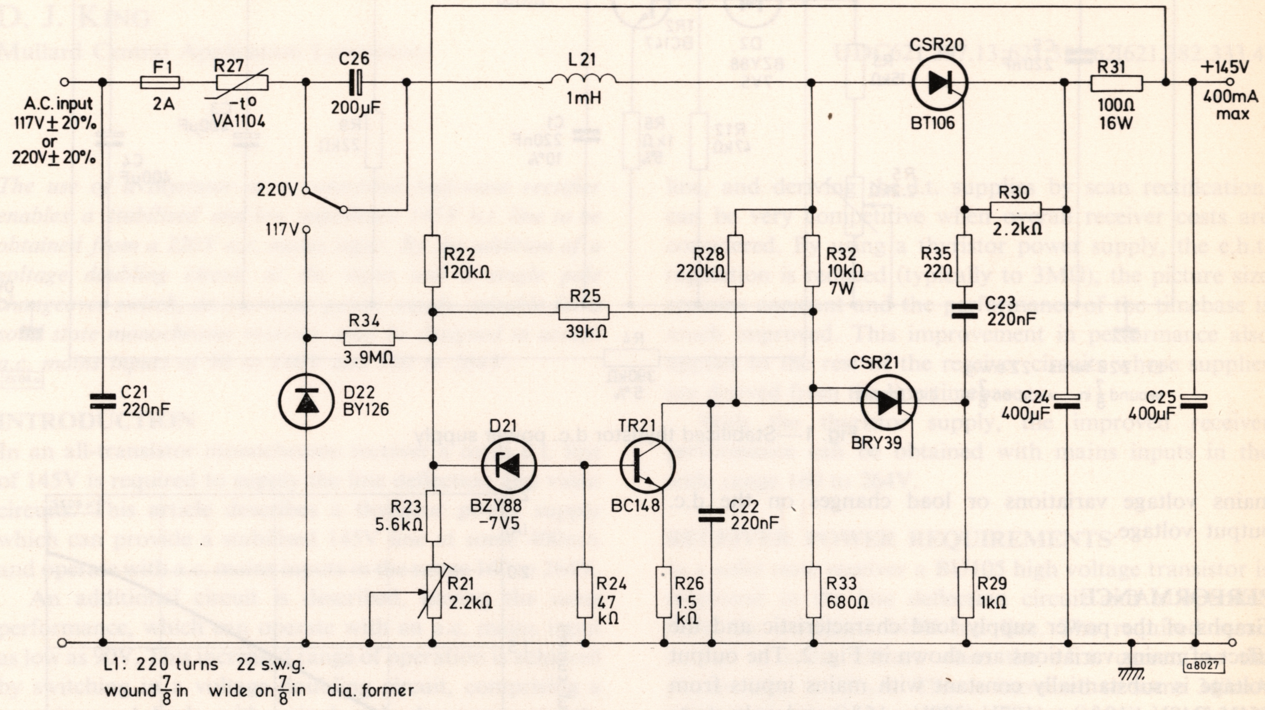

Fig. 4—Wide input range power supply

waveform is the silicon controlled switch BRY39. This is a four layer semiconductor device similar to a thyristor but with an anode gate terminal made available. The conditions for conduction with an SCS are that the anode must be more positive than the cathode, and further that the anode gate must be less positive than the anode.

To use the SCS to supply a pulse of current to trigger the thyristor CSR$_{20}$ in a stabilised power supply (Fig. 4), the delayed waveform from C$_{22}$ is applied to the anode. A sample of the clamped input waveform from a potential divider is then supplied to the anode gate.

The delay time-constants are arranged so that the trigger point is controlled to occur along the falling slope of this waveform and takes place when the delayed voltage on the anode rises above the falling anode gate voltage. The triggering voltage is obtained from the cathode of the SCS and applied to the thyristor gate. After triggering, the SCS continues in conduction causing C$_{22}$ to be discharged as the anode follows the sampled input waveform on the anode gate down to zero.

The complete power supply for a monochrome receiver, shown in Fig. 4, is designed to provide a stabilised 145V smoothed d.c. output from mains inputs of 90 to 140V. Provision is also made for operation from mains inputs of 160 to 264V by means of a simple single pole changeover switch. A graph of the overall performance characteristic is shown in Fig. 5.

It is possible to design this type of power supply to operate from 90 to 264V mains inputs, but such a design would require the voltage doubler to be left in the circuit. With the maximum mains input the output from the doubler would be some 750V. This would require an increase in the ratings of many components and devices which would inevitably be more expensive.

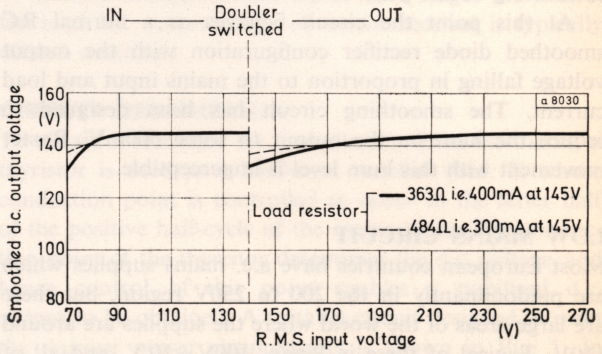

Fig. 5—Wide input range power supply characteristics

REFERENCES

1. ATTWOOD, B. E., 'Transistor Field Timebase for Colour and Monochrome Receivers'. **Mullard Technical Communications,** Vol. 9, No. 89, September 1967, pp. 246 to 251.
2. KING, D. J., 'Thyristor power supplies for colour tv receivers', **Mullard Technical Communications,** Vol. 11, No. 102. November 1969, pp. 29 to 34 (this issue).

Thyristor power supplies for colour tv receivers

D. J. KING
Mullard Central Application Laboratory

UDC 621.397.132:621.311.62[621.382.333.4]

This article, in two parts, describes stabilised thyristor power supply circuits designed for use in colour television receivers. Two types of circuit are considered: one which operates directly from the mains and one which incorporates a mains transformer to provide mains isolation.

The two sections of the article are as follows:

Part 1: Stabilised thyristor power supply.
Part 2: Isolated and stabilised thyristor power supply.

Part 1: Stabilised thyristor power supply

The article describes the use of a thyristor as a controlled half-wave rectifier to enable an h.t. potential of 200V to be obtained from a 220V a.c. mains input without the use of a transformer. A simple control circuit stabilises the d.c. output against mains potential variations and load changes. At very low mains potentials (220V–15%), good stabilisation is obtained using a short phase-shift time-constant in the triggering circuit of the thyristor. The output ripple is 500mV peak-to-peak and the movement of the raster with this level of hum is imperceptible.

This power supply technique enables an economical all-transistor television receiver to be produced that has a superior performance to its conventional hybrid counterpart in terms of stabilisation and heat dissipation.

INTRODUCTION

In an all-transistor colour television receiver, the line deflection and video output circuits require a stabilised 200V line at some 400mA. If this is supplied by a mains transformer, a very bulky and expensive component is required in addition to the stabilising circuit. A method of obtaining a stabilised 200V supply directly from the mains using a thyristor as a controlled half-wave rectifier is described in this article. By choosing the optimum control circuit parameters, excellent stabilisation can be achieved over a very wide range of mains input potentials. In addition, a high value smoothing resistor can be used to give good hum performance with the most economical size of smoothing capacitors.

The receiver field, audio and line driver stages, together with the signal processing circuits can be operated from a potential of about 40V. The total current required is about 1A. This supply can be derived either from a full-wave rectifier used in conjunction with a mains transformer or from the line output transformer by scan rectification.

A small mains transformer is required to supply the heater of the picture tube.

RECEIVER POWER REQUIREMENTS

In a conventional valve or hybrid receiver, the line deflection is stabilised by means of a v.d.r. feedback circuit, because the output valve is operated above the knee of its anode characteristic. This technique, however, results in additional anode dissipation.

In a transistor line deflection circuit, operation above the knee is not feasible because of the increased collector dissipation and resulting heatsink size. Hence, the transistors are operated as switches and bottomed when conducting, and the collector-base junctions can then be used as a shunt efficiency diode. In such a configuration, the peak voltage applied to the output device is approximately ten times the h.t. potential. However, a stabilised mode of operation is not possible with semiconductors, and to stabilise the deflection current and hence the picture size against mains input variations, a stabilised h.t. line must be used.

In the transistor line deflection circuit for a colour receiver, which is described in a companion article (Ref. 1), two series-connected BU105 transistors are employed, and operate from a stabilised 200V h.t. line. When the colour picture tube is operating at maximum beam current, the required mean current is some 350mA. The RGB video output stages, described in another article (Ref. 2), are also supplied from the 200V line, and this increases the load current by a further 60mA. Hence the stabilised supply has to provide an h.t. potential of 200V, with a load current varying between some 300 and 400mA with picture brightness. When the low potential stages are operated from a supply derived from the line output transformer, the line oscillator and driver must operate from the 200V line, and the total load current is then increased by 200mA to between 500 and 600mA.

To obtain this 200V line, a thyristor can be used in place of the normal diode rectifier, and its conduction point controlled to occur in the latter half of the positive half cycle of the mains input. In this way, a d.c. potential can be obtained that is less than the normal peak value of the a.c. input. The conduction point of the thyristor determines the d.c. potential, and hence control of this point enables a stabilised d.c. output to be obtained.

CIRCUIT DESCRIPTION

The basic circuit is shown in Fig. 1.1. The mains waveform is delayed by the phase-shift network R_5 and C_2, and applied to the trigger diac CSR_1*. When the potential across capacitor C_2 reaches the diac breakover potential, the diac conducts and a current pulse is applied to the gate of the thyristor causing it to conduct. Thus a simple power supply with an adjustable output can be obtained by making R_5 a variable resistor. Such a circuit, however, will not be stabilised.

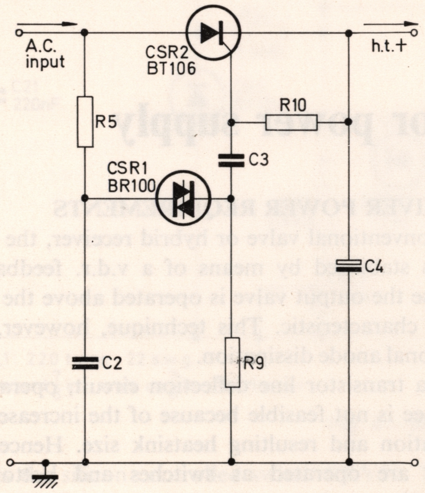

Fig. 1.1—Basic d.c. power supply using a thyristor triggered by a diac

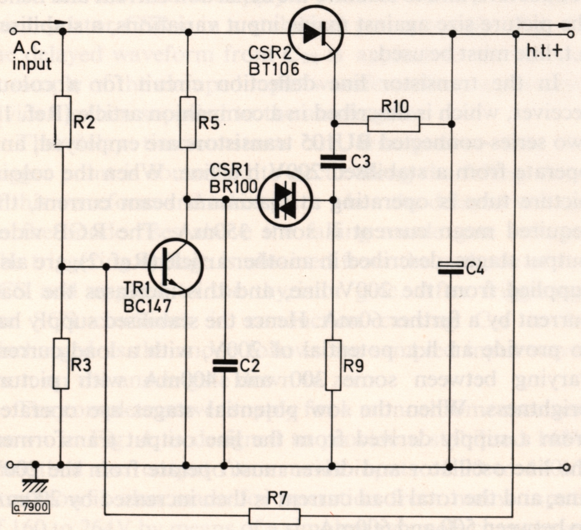

Fig. 1.2—Power supply of Fig. 1.1 stabilised against mains input and load variations

To stabilise the output, the trigger point must be varied as a function of mains input and d.c. output. A suitable circuit is shown in Fig. 1.2. The transistor is used to control the charge current of C_2, and hence the trigger point for the thyristor. The base of the transistor is connected to a potential divider across the mains input. If the input potential tends to increase, the base current is increased, and hence the charge current is reduced. This delays the trigger point and tends to maintain the output potential constant.

Additional feedback is provided by R_7 from the d.c. output. Again any tendency for the output to rise—for example, resulting from a change in load current—causes the base current of TR_1 to be increased, which reduces the charge current and delays the thyristor trigger point. Hence the effects of mains potential variations and load changes on the d.c. output potential are reduced to a minimum.

In this circuit configuration, the reference potential for the circuit is the V_{be} of the control transistor. Temperature variations cause large changes in the output potential, typically some −10% for an overall rise of 100°C in the junction temperature. This thermal effect can be eliminated by connecting a voltage reference diode D_1 in series with the base of the control transistor, as shown in Fig. 1.3. The preset resistor R_{12} is for the adjustment of the output potential to allow for component tolerances.

The thyristor has a fast turn-on time, typically 2 to 3μs, to minimise dissipation, and when it conducts in the cycle a high-current pulse flows because of the sudden application of the mains waveform to the reservoir capacitor C_4. As this would give rise to radio interference, an air-cored r.f. choke L_1 is necessary, and is connected in series with the thyristor together with a capacitor C_1 across the mains input. This network also protects the thyristor from possible damage caused by mains transients. The switch-on surge current of some 140A is reduced by the inclusion of a thermistor R_1 to protect the on/off switch.

The power supply has been designed to provide a 200V line at 300mA. For a colour receiver, the load current is expected to rise to some 400mA at maximum brightness and contrast. If the supply for the low potential stages is derived from the line output transformer, the line oscillator and driver must operate from the 200V potential. To supply this additional current, the component values of the circuit described can be modified to give 700mA as shown below:

R_1	2·2Ω, 20W, linear resistor
R_{11}	82Ω ± 5%, wirewound, 35W
Fuse	3A, delay type
L_1	820μH, 210 turns of 19 s.w.g. wound $\frac{7}{8}$ in wide on former diameter $\frac{3}{4}$ in.

PERFORMANCE

The h.t. line ripple at the output is about 500mV peak-to-peak, and the movement of the raster with this level of hum

---

*A diac is a bidirectional thyristor with no gate. Its characteristic has a negative resistance region which starts at a critical potential called the breakover voltage; for the BR100 this is nominally 32V.

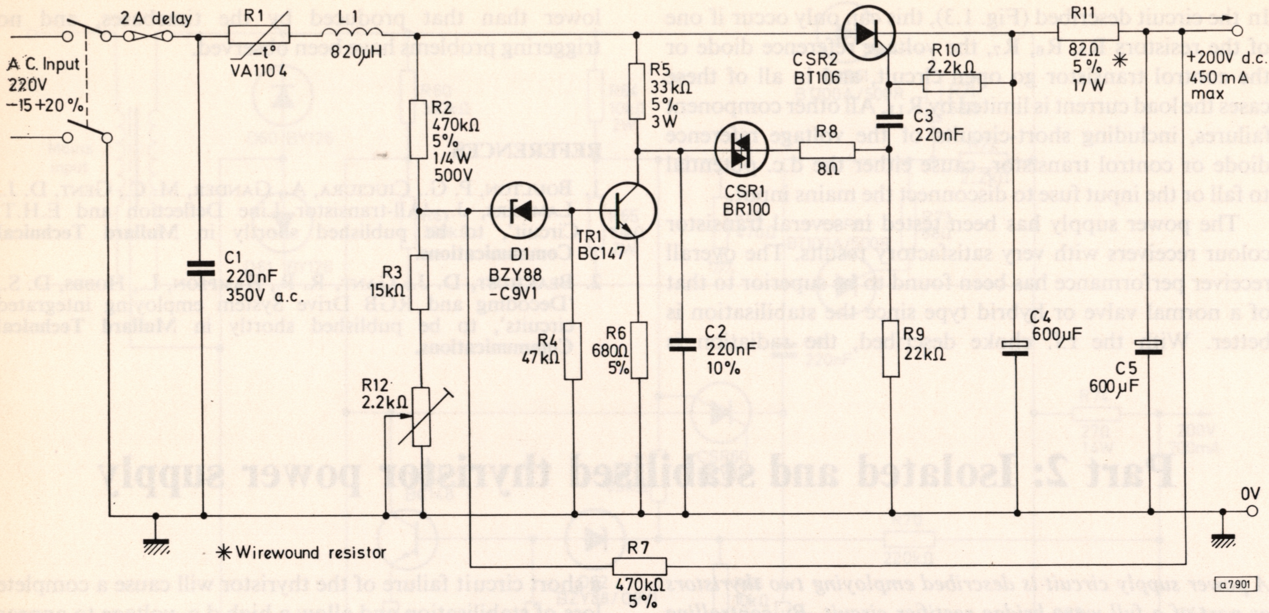

Fig. 1.3—Complete stabilised d.c. power supply

L_1: 210 turns of 21 s.w.g. wound $\frac{3}{4}$in wide on former, diameter $\frac{7}{8}$in.

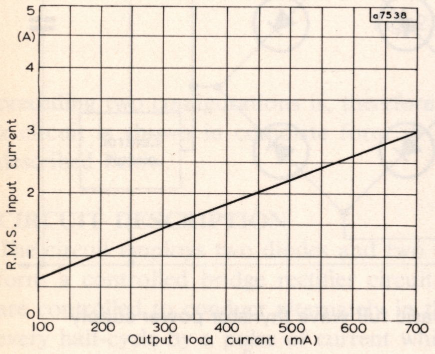

Fig. 1.4—Variation of r.m.s. input current with load current

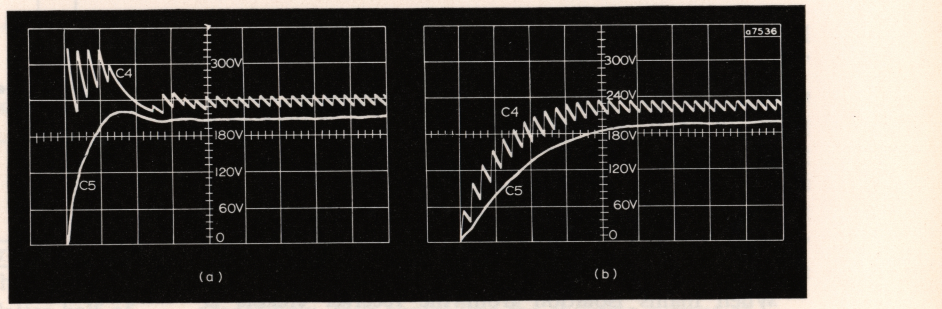

Fig. 1.5—Switch-on characteristics showing potentials at reservoir capacitor C_4 and smoothing capacitor C_5, at 50Hz mains

(a) without a current limiting thermistor (R_1)
(b) with thermistor VA1104

is imperceptible. Fig. 1.4 shows the variation of r.m.s. input current with load current. Since the conduction time of the thyristor is some 1·6ms, and is shorter than that of a normal diode circuit (2·4ms), this input current is some 50% greater. The switch-on waveforms of the power supply are shown in Fig. 1.5, both with and without a current-limiting thermistor.

With this type of power supply, no excessive heat is generated in the active devices, and it is possible, therefore, to design an economical circuit which can accept inputs from either the European 220V or U.K. 240V supplies. The maximum mains input will be 240V + 10% and the lowest normal value will be 220V −10%. Therefore, the circuit has been designed to accept an input voltage range of 198V to 264V whilst maintaining the output voltage to about −1% at both extremes. At −15% on 220V nominal mains (187V) the output voltage falls 2·5% which does not significantly affect the receiver. The power supply

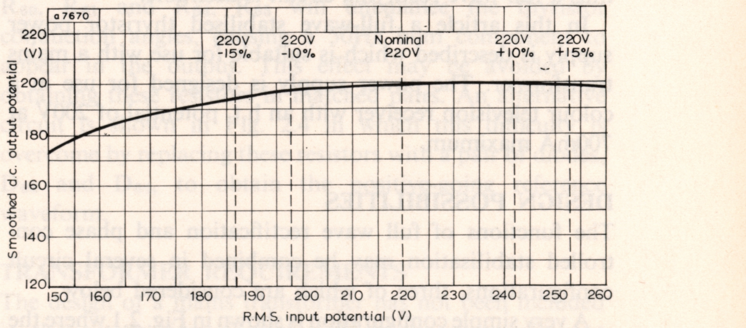

Fig. 1.6—Variation of output potential with input potential with 500Ω load resistance, (400mA at 200V)

characteristic is shown in Fig. 1.6. At low mains inputs the thyristor conducts on every positive half-cycle, and hence no discontinuity in the d.c. output characteristic occurs, even with very low mains input potentials.

The main danger from a stabilised power supply failure is that the output potential may exceed the normal value.

In the circuit described (Fig. 1.3), this can only occur if one of the resistors R_2, R_6, R_7, the voltage reference diode or the control transistor go open circuit, and in all of these cases the load current is limited by R_{11}. All other component failures, including short-circuits of the voltage reference diode or control transistor, cause either the d.c. potential to fall or the input fuse to disconnect the mains input.

The power supply has been tested in several transistor colour receivers with very satisfactory results. The overall receiver performance has been found to be superior to that of a normal valve or hybrid type since the stabilisation is better. With the r.f. choke described, the radiation is lower than that produced by the timebases, and no triggering problems have been observed.

REFERENCES

1. BOULTON, P. G., CIUCIURA, A., GANDER, M. C., GENT, D. J., LAMMERS, J., 'All-transistor Line Deflection and E.H.T. Circuit', to be published shortly in **Mullard Technical Communications.**
2. BEAKHUST, D. J., GANT, R. P., HAMPSON, L., HOBBS, D. S., 'Decoding and RGB Drive System employing integrated circuits', to be published shortly in **Mullard Technical Communications.**

Part 2: Isolated and stabilised thyristor power supply

A power supply circuit is described employing two thyristors as part of a full wave bridge rectifier circuit. By controlling the conduction point the smoothed output potential is stabilised at 200V. This supply unit is intended for use with a double wound mains transformer for applications where mains isolation is desirable or mandatory.

INTRODUCTION

The use of a stabilised power supply in an all-transistor colour television receiver has been described in Part 1, pages 29 to 32. In that circuit a thyristor is used as a phase controlled rectifier and a stabilised 200V h.t. line is produced directly from the supply mains with the minimum power dissipation. This technique employs half wave rectification and hence a d.c. component flows in the mains supply.

When mains isolation from the receiver chassis is required (as in school receivers and monitors) or in Australia where no d.c. component in the mains is allowed, a mains transformer is necessary. The half-wave circuit can be preceded by a suitable transformer but the d.c. component presents both design and stray field problems, thus a full-wave rectifying circuit is desirable.

In this article a full-wave stabilised thyristor power supply is described which is suitable for use with a mains transformer. The power supply is designed for use in a colour television receiver with an h.t. potential of 200V at 700mA maximum.

DESIGN POSSIBILITIES

The functions of full wave rectification and phase controlled stabilisation may be combined in several circuit configurations, three of which are considered below.

A very simple configuration is shown in Fig. 2.1 where the transformer output waveform is converted into a series of positive-going half-cycles by a bridge rectifier. This is applied to a thyristor whose conduction point is controlled to occur in the latter half of each half-cycle and thus provide a stabilised output.

Excellent performance can be obtained from this type of circuit and the peak voltage across the devices is minimum. Unlike the original half-wave circuit, however, a short circuit failure of the thyristor will cause a complete loss of stabilisation and allow a high d.c. voltage to appear at the output.

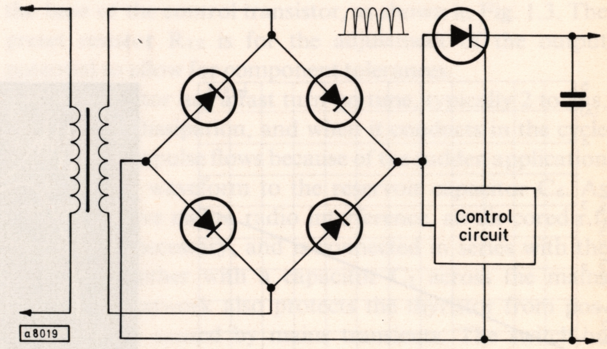

Fig. 2.1—Basic full wave thyristor power supply

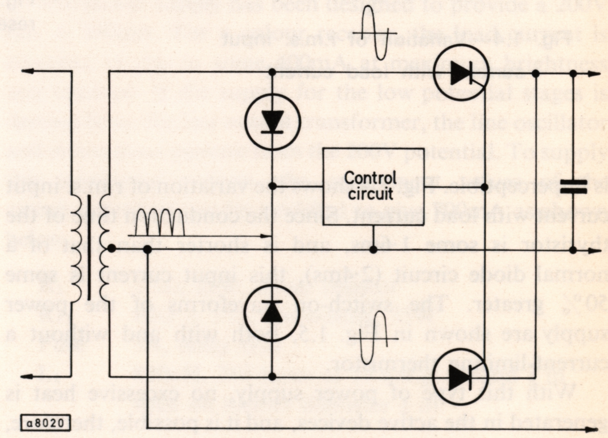

Fig. 2.2—Basic bi-phase thyristor power supply

This condition cannot occur in the bi-phase circuit shown in Fig. 2.2 but the mains transformer for this circuit will be larger and, therefore, more expensive. The peak voltage across all the main devices is also doubled.

A circuit which has none of the disadvantages of the preceding two configurations is, therefore, required. Such a circuit is shown in complete form in Fig. 2.3, and is described below.

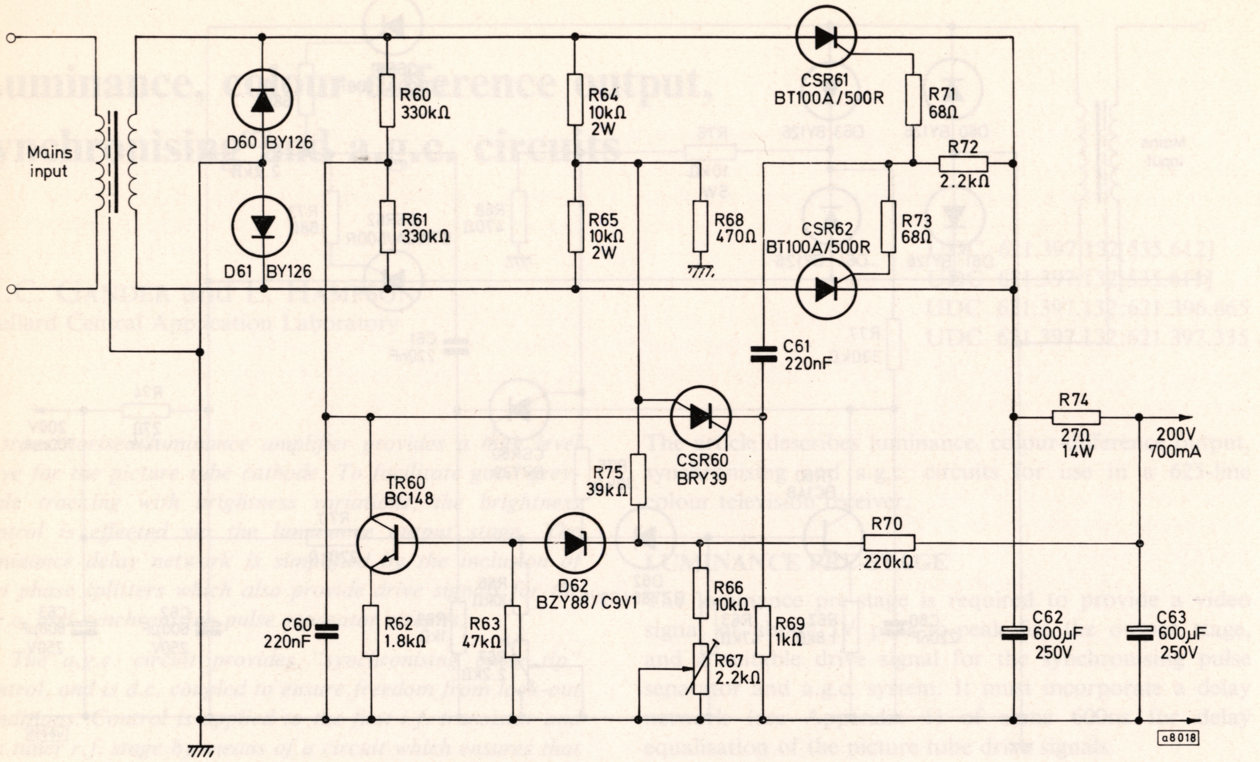

Fig. 2.3—Complete full wave thyristor power supply

CIRCUIT DESCRIPTION

The circuit employs two diodes and two thyristors which form a controlled bridge rectifier circuit. The thyristors are controlled to conduct alternately in the latter half of every half-cycle by a pulse of current which is applied to both thyristor gates simultaneously every half-cycle. Although this trigger pulse is applied to both thyristors only the one whose anode is positive at that instant will conduct. The anode of the other thyristor would at this moment be negative and, therefore, remain non-conductive until the next half-cycle.

To obtain a trigger pulse every half-cycle, the mains transformer output waveform must be converted into a series of positive-going half-cycles before it is supplied to the control transistor and trigger device. A suitable waveform may be obtained at the junction of R_{60} and R_{61} because of the alternate conduction of diodes D_{60} and D_{61}. The waveform is then delayed in phase by C_{60} and applied to a suitable trigger device. Since the waveform has a mean d.c. value a silicon control switch is required as a triggering device (Ref. 1).

The delayed waveform from C_{60} is supplied to the anode of CSR_{60} and a sample of the non-delayed waveform, obtained from R_{64}, R_{65}, is applied to the anode gate. The delay time-constants are arranged so that the trigger point occurs along the falling slope of this waveform and takes place when the delayed potential on the anode rises above the falling anode gate voltage. The triggering potential is obtained from the cathode of CSR_{60} and applied to the thyristor gates.

Transistor TR_{60} is used to control the charging current of C_{60} and hence the trigger point for the thyristors. The base circuit of the transistor is connected to a potential divider across the transformer output which senses changes in mains input and varies the base current accordingly, thus controlling the charging current of C_{60}. Feedback from the d.c. output is also applied to the transistor by R_{70} and any tendency for changes in output voltage, due for example to load current variations, is again controlled.

An adverse combination of tolerances in resistors R_{60}, R_{61} and R_{64}, R_{65} will unbalance the thyristor conduction angles, causing a 50Hz hum component to appear in the output. This effect may be avoided by obtaining these resistors in matched pairs. An alternative circuit is shown in Fig. 2.4 in which this difficulty is overcome by replacing these resistors with a pair of diodes, D_{63} and D_{64}, to obtain the positive-going reference waveform.

TRANSFORMER REQUIREMENTS

The design of a mains transformer has not been included in this article since factors such as the range of input voltages to be covered and operating ambient temperatures will influence the design and depend largely on the equipment designer's requirements. Some parameters influencing the transformer design can, however, be outlined.

For a stabilised h.t. line of 200V with a mains input range of ±10%, the secondary output voltage required

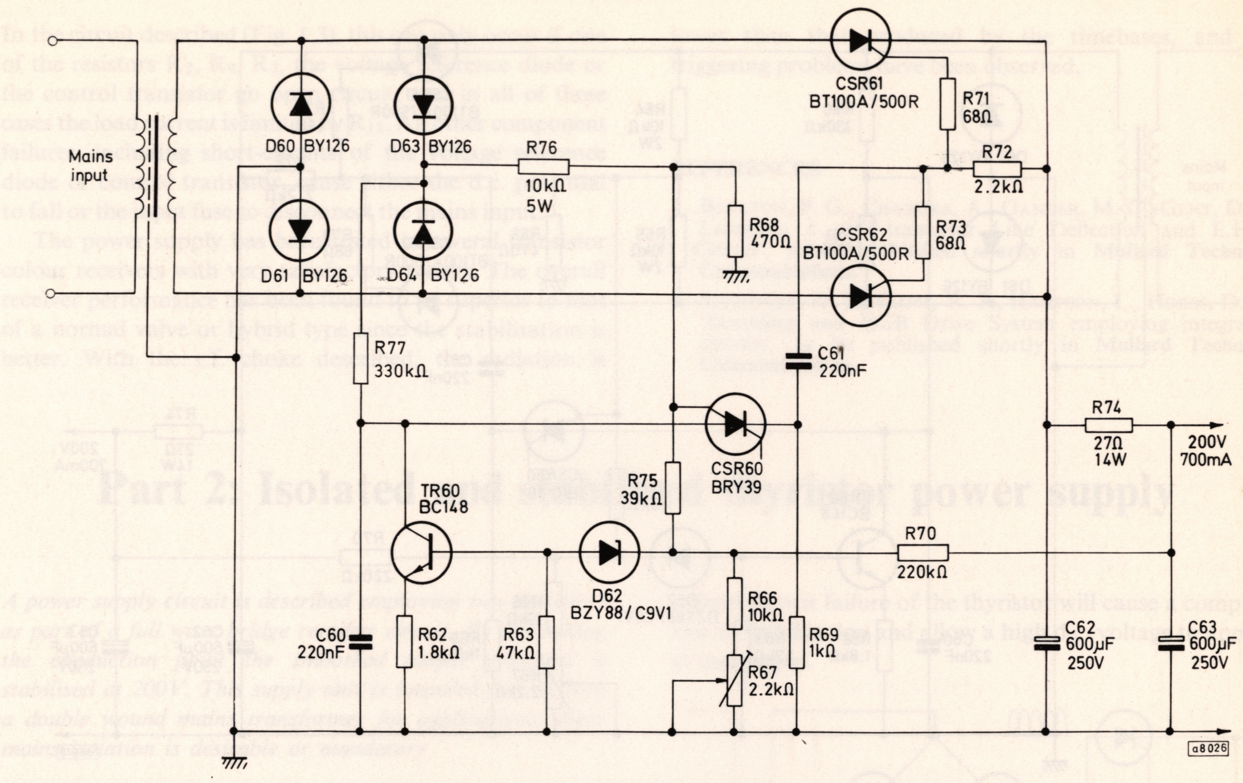
Mains input
D60 BY126
D61 BY126
D63 BY126
D64 BY126
R76 10kΩ 5W
R77 330kΩ
R68 470Ω
CSR61 BT100A/500R
R71 68Ω
R72 2.2kΩ
CSR62 BT100A/500R
R73 68Ω
C61 220nF
CSR60 BRY39
R74 27Ω 14W
200V 700mA
R75 39kΩ
TR60 BC148
R70 220kΩ
D62 BZY88/C9V1
R66 10kΩ
R67 2.2kΩ
R69 1kΩ
C60 220nF
R62 1.8kΩ
R63 47kΩ
C62 600μF 250V
C63 600μF 250V
a8026

Fig. 2.4—Alternative power supply configuration

would be 180V r.m.s. With this output voltage, the transformer's secondary+reflected primary resistance should total 7Ω minimum to limit the maximum surge current in a thyristor to less than 40A. A minimum leakage inductance of 1mH together with a screened primary would ensure that radio interference is suppressed to within accepted limits. Hence in the circuit (Fig. 2.3) no suppression inductance or n.t.c. resistor is shown.

REFERENCE

1. King, D. J., 'Monochrome tv power supplies for 117 and 220V mains inputs', **Mullard Technical Communications**, Vol. 11, No. 102, November 1969, pp. 26 to 28 (this issue).

MULLARD TECHNICAL COMMUNICATIONS

Vol. 11, No. 101, September 1969

Page 8

The final expression in the last sentence in the section *Common mode and supply rejection ratios* should read

$$\frac{1}{g_{fs(1b)}} - \frac{1}{g_{fs(1a)}}$$

Page 9

Following Eq.17, the assumed value of V_p should read

$$(V_{p(1a)} + V_{p(1b)})/2$$

Page 16

On the right-hand side of the first statement of Eq.26, the initial negative sign applies to the entire fraction and not to the first term of the numerator only.

Luminance, colour-difference output, synchronising and a.g.c. circuits

M.C. Gander and L. Hampson
Mullard Central Application Laboratory

UDC 621.397.132[535.612]
UDC 621.397.132[535.611]
UDC 621.397.132:621.396.665
UDC 621.397.132:621.397.335

A transistorised luminance amplifier provides a high level drive for the picture tube cathode. To facilitate good grey-scale tracking with brightness variations, the brightness control is effected via the luminance output stage. The luminance delay network is simplified by the inclusion of two phase splitters which also provide drive signals for the a.g.c. and synchronising pulse separator circuits.

The a.g.c. circuit provides "synchronising pulse tip" control, and is d.c. coupled to ensure freedom from lock-out conditions. Control is applied to the first i.f. transistor and the tuner r.f. stage by means of a circuit which ensures that the tuner gain is not reduced until the full i.f. control has been applied.

A single-transistor synchronising pulse separator is driven from a phase splitter, and its output drives the valve timebases directly. "High-level" contrast control is used and hence the receiver synchronisation is unaffected by brightness or contrast variations. The mean picture tube beam current is limited by a simple circuit which reduces the effect on the picture of maladjustment of the brightness or contrast controls.

The article describes luminance, colour-difference output, synchronising and a.g.c. circuits for use in a 625-line colour television receiver.

LUMINANCE PRE-STAGE

The luminance pre-stage is required to provide a video signal of about 5V peak-to-peak for the output stage, and a suitable drive signal for the synchronising pulse separator and a.g.c. system. It must incorporate a delay network (see Appendix 1) of some 600ns for delay equalisation of the picture tube drive signals.

Circuit description

The circuit diagram of the luminance pre-stage is shown in Fig. 1. The video detector drives the phase-splitter transistor TR_{106}. Luminance signals are taken from its collector via the luminance delay network which comprises a continuously-wound delay line having an impedance of 1kΩ, terminated at both ends. The constructional and performance details are given in Appendix 1. The collector network includes a trap tuned to the

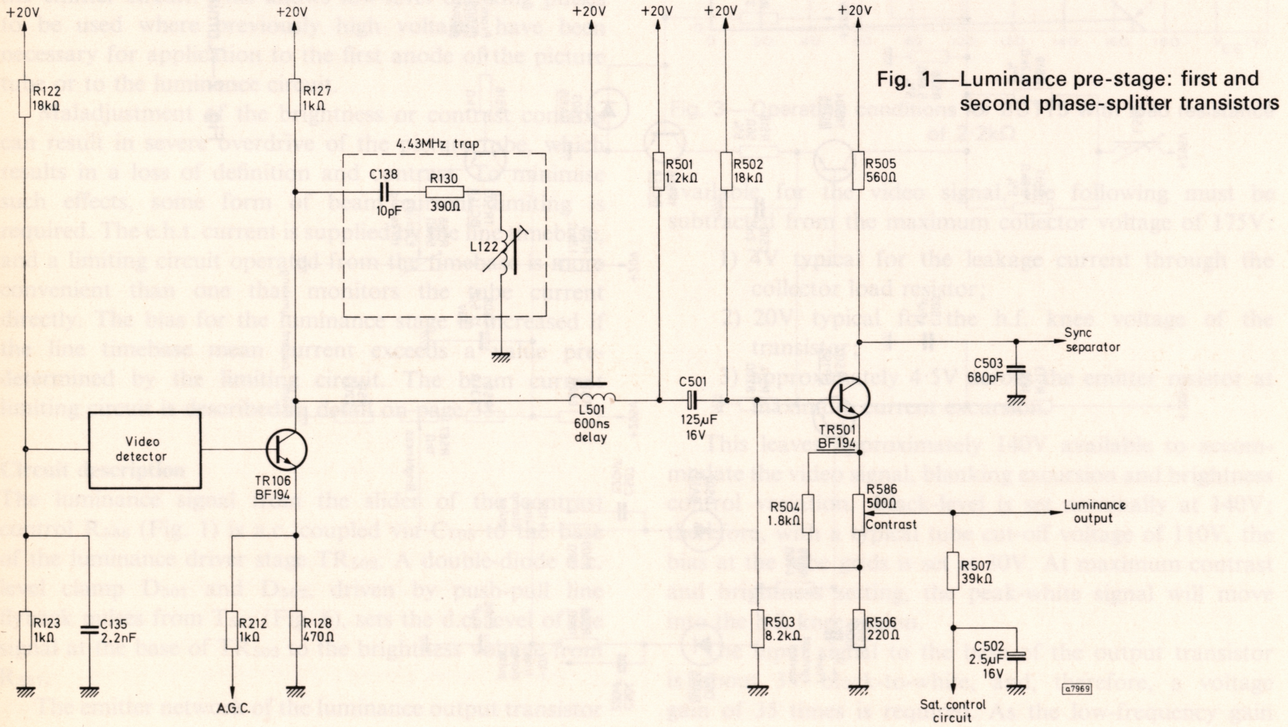
+20V
R122 18kΩ
R127 1kΩ
4.43MHz trap
C138 10pF
R130 390Ω
L122
L501 600ns delay
C501 125μF 16V
R501 1.2kΩ
R502 18kΩ
R505 560Ω
Sync separator
C503 680pF
TR501 BF194
Video detector
TR106 BF194
R504 1.8kΩ
R586 500Ω
Contrast
Luminance output
R507 39kΩ
R123 1kΩ
C135 2.2nF
R212 1kΩ
R128 470Ω
A.G.C.
R503 8.2kΩ
R506 220Ω
C502 2.5μF 16V
Sat. control circuit
a7969

Fig. 1—Luminance pre-stage: first and second phase-splitter transistors

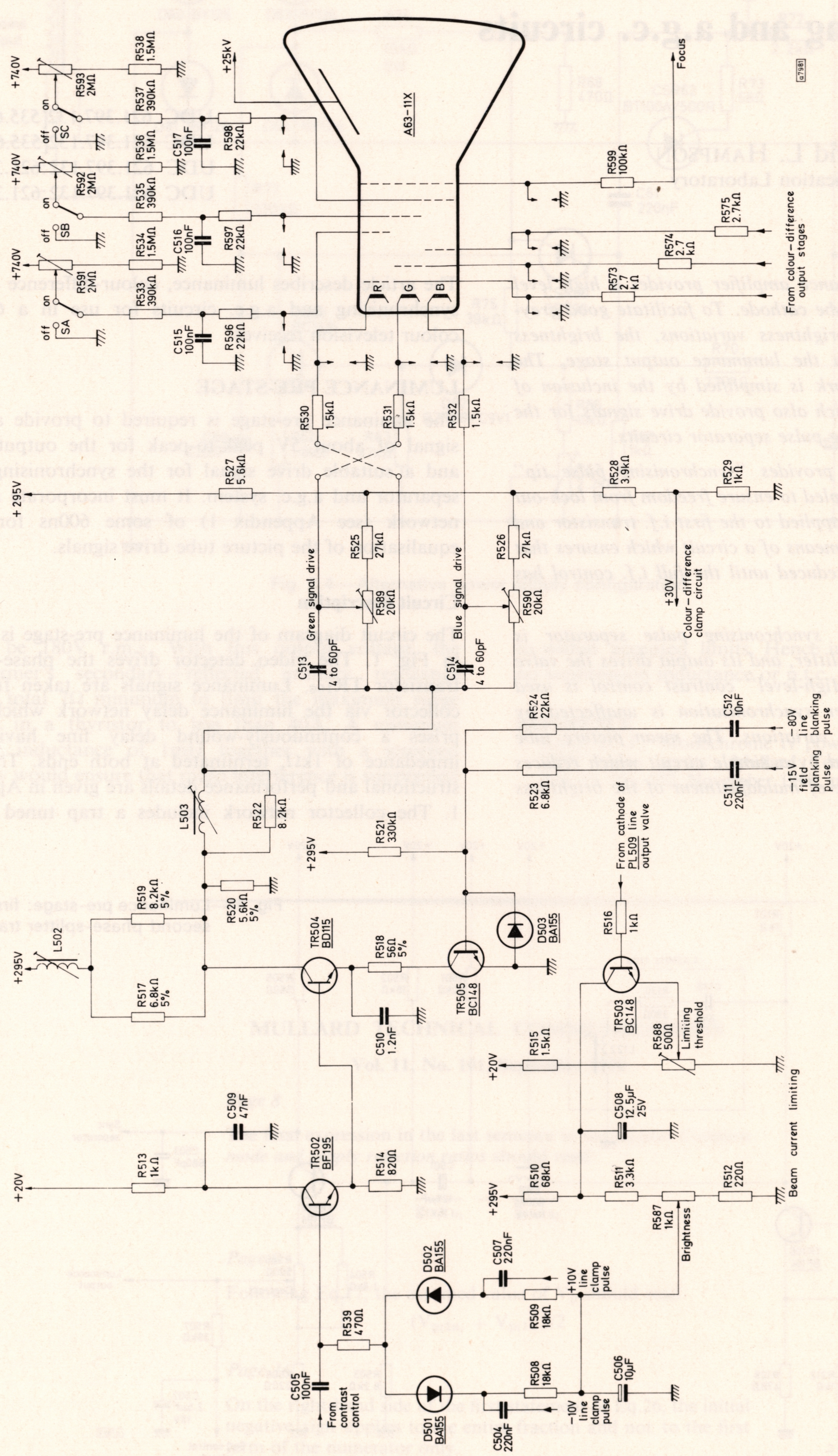
+740V
R593 2MΩ
R538 1.5MΩ
R537 390kΩ
+25kV
on
off
SC
R536 1.5MΩ
C517 100nF
R598 22kΩ
A63-11X
Focus
R592 2MΩ
R535 390kΩ
SB
R534 1.5MΩ
C516 100nF
R597 22kΩ
R599 100kΩ
R575 2.7kΩ
R574 2.7kΩ
R573 2.7kΩ
R591 2MΩ
R533 390kΩ
SA
C515 100nF
R596 22kΩ
R
G
B
From colour-difference output stages
R530 1.5kΩ
R531 1.5kΩ
R532 1.5kΩ
R527 5.6kΩ
R525 27kΩ
R528 3.9kΩ
R529 1kΩ
R526 27kΩ
Green signal drive
Blue signal drive
R589 20kΩ
R590 20kΩ
+30V
Colour-difference clamp circuit
C513 4 to 60pF
C514 4 to 60pF
R524 22kΩ
C512 10nF
−80V line blanking pulse
R523 6.8kΩ
C511 220nF
−15V field blanking pulse
R522 8.2kΩ
L503
+295V
R521 330kΩ
From cathode of PL509 line output valve
R519 8.2kΩ 5%
R520 5.6kΩ 5%
+295V
L502
TR504 BD115
R518 56Ω 5%
D503 BA155
R516 1kΩ
R517 6.8kΩ 5%
TR505 BC148
TR503 BC148
C510 1.2nF
R515 1.5kΩ
R588 500Ω
Limiting threshold
+20V
C509 47nF
C508 12.5μF 25V
TR502 BF195
+20V
R513 1kΩ
R514 820Ω
+295V
R510 68kΩ
R511 3.3kΩ
R512 220Ω
Beam current limiting
R587 1kΩ
Brightness
D502 BA155
C507 220nF
+10V line clamp pulse
R539 470Ω
R509 18kΩ
C505 100nF
From contrast control
R508 18kΩ
C506 10μF
D501 BA155
C504 220nF
−10V line clamp pulse

Fig. 2—Luminance output, picture tube drive, and beam current limiting circuits

colour subcarrier frequency (4·43MHz) which reduces the amplitude of the subcarrier signal fed into the luminance delay line.

The drive for the a.g.c. system is taken from the emitter of the phase-splitter via R$_{212}$. The a.g.c. circuit is described in detail on pages 40 to 41.

A low-impedance high-level contrast control is desirable because it enables the picture contrast to be varied independently of the synchronising and a.g.c. circuits. Furthermore, the termination of the luminance delay network is simplified if a capacitive load can be avoided. A second phase-splitter TR$_{501}$ is therefore used, with the synchronising pulse separator driven from its collector, and the contrast control from its emitter. The signal from the slider of the contrast control is a.c. coupled into a black-level clamp circuit, and is then taken to the luminance output stage.

LUMINANCE OUTPUT STAGE

A BD115 transistor used in the luminance output stage (Fig. 2) is able to provide the high luminance drive required by a colour picture tube with adequate bandwidth and stability. The operating conditions have been chosen to limit the maximum collector dissipation to 4W to keep the heatsink to a manageable size. A collector supply voltage of 175V is derived by means of a potential divider from the main h.t. line of 295V (nominal) with a collector load of 2·2kΩ. It is thus possible to deliver a black-to-white video signal of 105V together with 15V blanking excursion and 20V d.c.-level variation for brightness control.

Potentiometer feed to the picture tube is achieved by two 20kΩ potentiometers (green and blue guns) and a fixed black-level reference divider between the h.t. supply line and chassis.

Blanking is applied by means of a series transistor in the emitter circuit. This allows low-level blanking pulses to be used where previously high voltages have been necessary for application to the first anode of the picture tube or to the luminance circuit.

Maladjustment of the brightness or contrast controls can result in severe overdrive of the picture tube, which results in a loss of definition and contrast. To minimise such effects, some form of beam current limiting is required. The e.h.t. current is supplied by the line timebase, and a limiting circuit operated from the timebase is more convenient than one that monitors the tube current directly. The bias for the luminance stage is increased if the line timebase mean current exceeds a value predetermined by the limiting circuit. The beam current limiting circuit is described in detail on page 38.

Circuit description

The luminance signal from the slider of the contrast control R$_{586}$ (Fig. 1) is a.c. coupled via C$_{505}$ to the base of the luminance driver stage TR$_{502}$. A double-diode d.c. level clamp D$_{501}$ and D$_{502}$, driven by push-pull line flyback pulses from T$_{501}$ (Fig. 6), sets the d.c. level of the signal at the base of TR$_{502}$ to the brightness voltage from R$_{587}$.

The emitter network of the luminance output transistor TR$_{504}$ contains a low-level blanking stage TR$_{505}$. During the picture period, TR$_{505}$ is held bottomed by the current fed into its base via R$_{521}$, and its collector saturation resistance under this condition is about 20Ω. Negative-going line and field flyback pulses are fed to the base of TR$_{505}$ via C$_{511}$ and C$_{512}$, and these cut off the blanking transistor and thereby also the output transistor. Diode D$_{503}$ prevents reverse breakdown of the base-emitter junction of TR$_{505}$.

The collector of the luminance output transistor TR$_{504}$ is supplied from a network of resistors giving a collector supply voltage of 175V with an h.t. supply voltage of 295V nominal. If resistors with a tolerance of ±5% are used in the collector network, the maximum dissipation of 4W for the BD115 will not be exceeded provided that the collector supply voltage does not rise above 190V; that is, the main h.t. line does not exceed 330V. The thermal resistance of the heatsink should not exceed 20degC/W. This will permit adequate cooling for ambient temperatures not exceeding 55°C.

Fig. 3 shows the operating conditions for the BD115 with a 2·2kΩ load resistance. To calculate the voltage

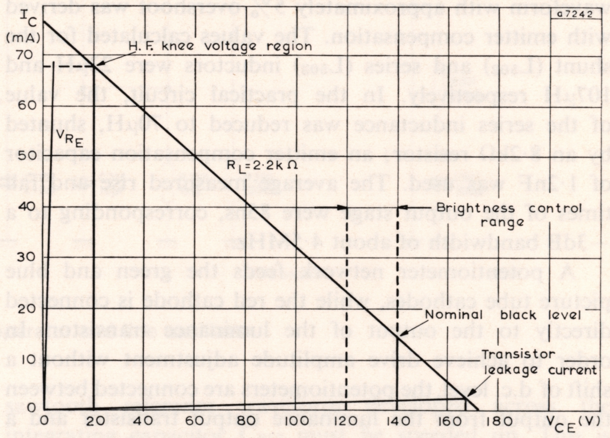

Fig. 3—Operating conditions for BD115 with load resistance of 2·2kΩ

available for the video signal, the following must be subtracted from the maximum collector voltage of 175V:

1) 4V typical for the leakage current through the collector load resistor;
2) 20V typical for the h.f. knee voltage of the transistor;
3) approximately 4·5V across the emitter resistor at maximum current excursion.

This leaves approximately 140V available to accommodate the video signal, blanking excursion and brightness control variation. Black-level is set nominally at 140V; therefore, with a typical tube cut-off voltage of 110V, the bias at the tube grids is set at 30V. At maximum contrast and brightness setting, the peak-white signal will move into the h.f. knee region.

The input signal to the base of the output transistor is about 3V black-to-white, and, therefore, a voltage gain of 35 times is required. As the low-frequency gain is closely determined by the ratio of collector load resistance to emitter resistance, the value of the latter will be about 65Ω. Because allowance must be made for the resistance of the bottomed blanking transistor, a 56Ω, 5% tolerance resistor is used.

To achieve the video bandwidth required in the output stage, normal h.f. compensation is required. In an uncompensated amplifier with a 2·2kΩ collector load, the measured rise time (10% to 90%) was 240ns, corresponding to a −3dB bandwidth of 1·46MHz. This corresponds to a total shunt capacitance of 48pF, which consists of:

1) transistor output capacitance, plus heatsink capacitance:	11pF
2) self-capacitance of collector load resistors, plus stray wiring capacitance:	5pF
3) input capacitance of picture tube cathodes:	17pF
4) capacitance of drive potentiometer system:	15pF

The ratio of items (1 and 2) to (3 and 4) is arranged to be 1:2 in accordance with design formulae (Ref. 1). To obtain the optimum frequency response, the values of shunt and series inductances were derived for an approximately "linear-phase" condition, and the final output waveform with approximately 5% overshoot was derived with emitter compensation. The values calculated for the shunt (L_{502}) and series (L_{503}) inductors were 23μH and 107μH respectively. In the practical circuit, the value of the series inductance was reduced to 70μH, shunted by an 8·2kΩ resistor; an emitter compensation capacitor of 1·2nF was used. The average measured rise and fall times of the output stage were 85ns, corresponding to a −3dB bandwidth of about 4·5MHz.

A potentiometer network feeds the green and blue picture tube cathodes, while the red cathode is connected directly to the output of the luminance transistor. In order to achieve drive amplitude adjustment without a shift of d.c. level, the potentiometers are connected between the output from the luminance output transistor and a fixed voltage divider R_{527}, R_{528} and R_{529}. This supplies a voltage of +140V, which is equal to the drive-signal black-level. Low-value trimmer capacitors C_{513} and C_{514}, connected across the drive potentiometers, compensate for loss of drive at h.f.

The first anodes of the picture tube are supplied from the boost voltage of the line timebase, described in Ref. 2, by means of a resistor and smoothing capacitor. The required first anode voltage range is +220 to +520V but, because the cathodes are at +140V at black-level, a range of +360 to +660V is actually necessary. Operation of switches S_A, S_B and S_C removes the first anode potentials for adjustment purposes. Spark gaps must be connected between each electrode and the picture tube external coating, and are used in conjunction with isolating resistors to protect the external circuitry against picture tube flashover effects. The grey-scale adjustments are described in Appendix 2.

BEAM CURRENT LIMITING CIRCUIT

The published data for the A63-11X and the A49-11X colour picture tubes specify that the short-term mean total current for the tubes should be limited to 1·5mA and 1·1mA respectively. Furthermore, the operation of the receiver controls is easier for the user, and overloading of the e.h.t., line timebase and h.t. circuits can be prevented by including a means of limiting the picture tube beam current.

In a receiver employing a multiplier type of e.h.t. supply circuit driven from the line output valve, there is a sufficiently good correlation between the e.h.t. mean current and the mean cathode current of the line output valve to employ the latter to operate a beam current limiting circuit.

Circuit description

A simple circuit which limits the e.h.t. current, whichever circuit is over-driving the picture tube, is shown in Fig. 2. For low e.h.t. currents, transistor TR_{503} is cut off by the voltage at its emitter from R_{588}. The base of TR_{503} is supplied from a decoupled 10Ω resistor in the cathode load of the line output valve so that, when the voltage across the cathode resistor exceeds the voltage supplied from R_{588}, the transistor starts to conduct. Its collector is connected into the brightness control network so that the picture tube brightness level is reduced if the e.h.t. current exceeds the value which is predetermined by the setting of R_{588}.

This control technique has no effect upon the operation of the receiver while the mean beam current is below the limiting threshold level because the feedback loop is open. In the event of maladjustment of the receiver controls, or an excessive increase in the picture content mean level, or any combination of these, the mean beam current is effectively limited. A further benefit of the circuit is that it effectively provides an electrical "end stop" on the range of the brightness control, which eases the problem of tolerances in the brightness control network. The time-constant of the feedback loop is made sufficiently long by C_{508} to avoid oscillation and prevent any limiting of low duty-cycle picture highlights.

SYNCHRONISING PULSE SEPARATOR AND LINE OSCILLATOR

The synchronising pulse separator and line oscillator in a colour receiver perform similar functions to their counterparts in a monochrome receiver. The separator is driven from a low-level signal source, and a transistor is used for the separator.

Circuit description

The synchronising pulse separator and line oscillator circuit are shown in Fig. 4. A BC147 transistor TR_{204} is employed as the separator, operating with a collector potential derived from the 220V line. This enables a synchronising waveform to be obtained directly from the separator transistor, having sufficient amplitude to drive the flywheel phase detector and field separator.

A composite video waveform of 5V peak-to-peak amplitude is developed across the collector resistor R_{505} of the second luminance phase-splitter transistor TR_{501} (Fig. 1) to drive the synchronising pulse separator. The stray capacitance at the emitter due to the screened wiring to the contrast control R_{586} causes h.f. overshoot at the collector. Compensation for this effect is made by the shunt capacitor C_{503} in the collector circuit.

The collector waveform of the phase-splitter transistor is taken to the base of the separator TR_{204} via a long-time-constant a.c. coupling C_{205}, R_{214} which, because of the base current flowing during the synchronising pulse tips, reverse-biases the base of the separator in the conventional way. Resistor R_{213} supplies a small forward-bias current to ensure that the separator collector bottoms satisfactorily during the synchronising pulse tips with video signals having a low average level. A diode D_{202} with a low forward impedance is included in the emitter circuit to safeguard the transistor against base-emitter breakdown due to surges caused by abnormal operating conditions.

The pentode section of the PCF802 operates as a screen-coupled Hartley oscillator with the line drive developed at its anode. The triode section of the valve functions as a variable capacitive-reactance element. A quadrature sinewave which is developed across the resistor R_{229} connected in series with the tuned-circuit capacitor C_{218} is applied to the triode grid via C_{217}.

The double-diode phase detector is driven via C_{207} from the collector of the synchronising pulse separator. The coupling capacitor C_{207} is kept to a low value to minimise the field pulse group disturbance in the flywheel system, which may otherwise appear as a horizontal displacement at the top of the picture, and also to reduce the sensitivity of the flywheel to low-frequency noise or interference on the incoming signal. A sawtooth phase-reference waveform having an amplitude of approximately 25V peak-to-peak is developed by integration (R_{218}, C_{213}) of a flyback pulse of approximately 750V peak amplitude obtained from a tap on the line output transformer. The phase detector should operate with an output potential of nominally zero volts at phase centre. To obtain this condition the negative-going edge of the sawtooth reference waveform developed across the integrating capacitor C_{213} must be speeded up. This is achieved by connecting capacitor C_{211} across the main sawtooth integrating resistor R_{218}. By connecting R_{222} in series with the input flyback pulse, the phase-detector diodes are protected against large-amplitude pulses, which may be introduced into the line output transformer as a result of picture tube flashover.

This simple form of phase detector has the disadvantage that, in the absence of the synchronising waveform, diode rectification of the sawtooth waveform occurs through D_{203} and C_{207}, and results in a small residual positive charge on C_{207} which appears, via R_{220}, at the output of the phase detector. This has the effect of sending the line oscillator off its correct frequency, and consequently the pull-in range is not situated symmetrically about the centre frequency. This imbalance can be minimised by keeping C_{207} to a low value, but extra correction can be made by connecting a small capacitor C_{212} across diode D_{203}. The diode is caused to conduct by the reference waveform, and a charge is produced on C_{212} which opposes the charge on C_{207}. By a suitable proportioning of C_{212} and C_{207}, the residual imbalance can be appreciably reduced.

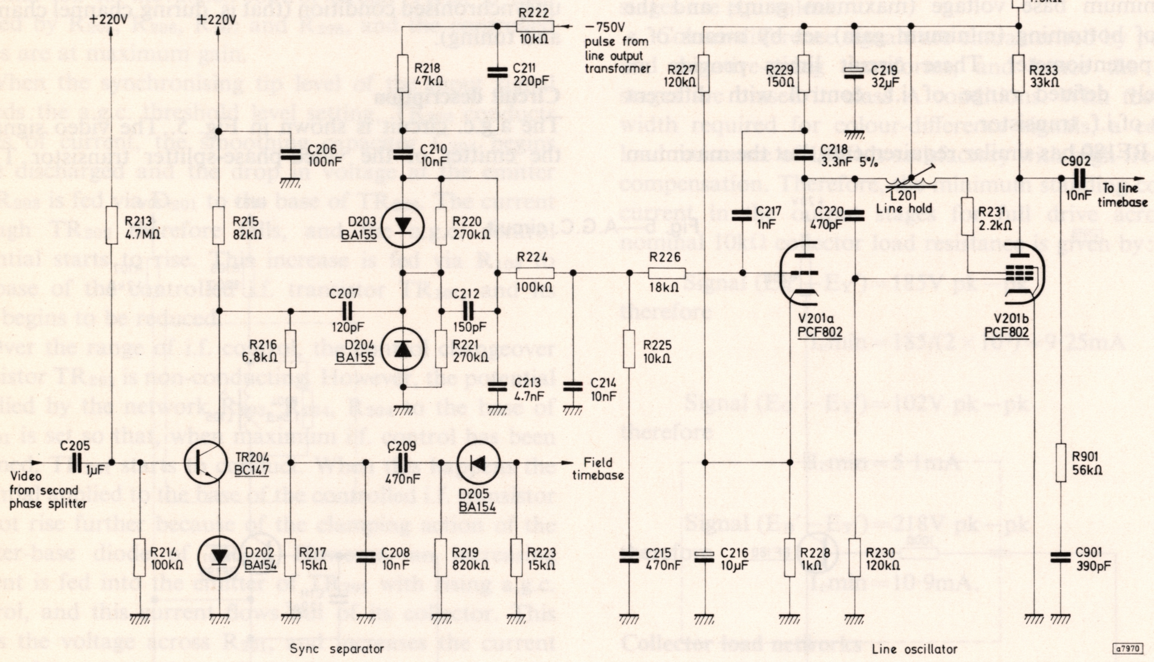

Fig. 4—Synchronising pulse separator and line oscillator

A.G.C. CIRCUIT

The automatic gain control requirements for the i.f. amplifier, described in Ref. 3, are determined by the control characteristics of the first i.f. transistor (BF196) and the tuner r.f. transistor (BF180).

The BF196 is operated over a current range of 4 to 10mA to provide a forward gain control of approximately 50dB. The mode of operation is partly current control and partly voltage control, and calls for a low-impedance a.g.c. circuit. The limits of the control range are fixed by: the correct choice of emitter-bias-chain components; the minimum base voltage (maximum gain); and the extent of bottoming (minimum gain) set by means of a preset potentiometer. These circuit limits provide an accurately defined range of i.f. control with different samples of i.f. transistor.

The BF180 has similar requirements, but the maximum control need not be defined. The major requirement is to ensure that the mixer stage is not overloaded by the signal as a result of too large an i.f. gain reduction before the transfer of control.

Detection of the amplitude of the synchronising pulse tips in the video signal for a.g.c. purposes is convenient in the negative-modulation system. This system, d.c. coupled, operates on a peak-detection principle when "in tune", but on a mean-level principle when "tuning in". This avoids the possibility of signal "lock-out" which can occur in gated systems when the receiver is operating in an unsynchronised condition (that is, during channel changing and tuning).

Circuit description

The a.g.c. circuit is shown in Fig. 5. The video signal at the emitter of the video-phase-splitter transistor TR$_{106}$ is d.c. coupled to the base of the peak detector transistor TR$_{203}$. A reference bias is applied to the emitter of TR$_{203}$ from the voltage divider R$_{210}$ and R$_{235}$. When the level of the synchronising pulse tips on the video detector output signal exceeds this bias by about 1V, a.g.c. control begins. Thus R$_{235}$ functions as the a.g.c. threshold level control.

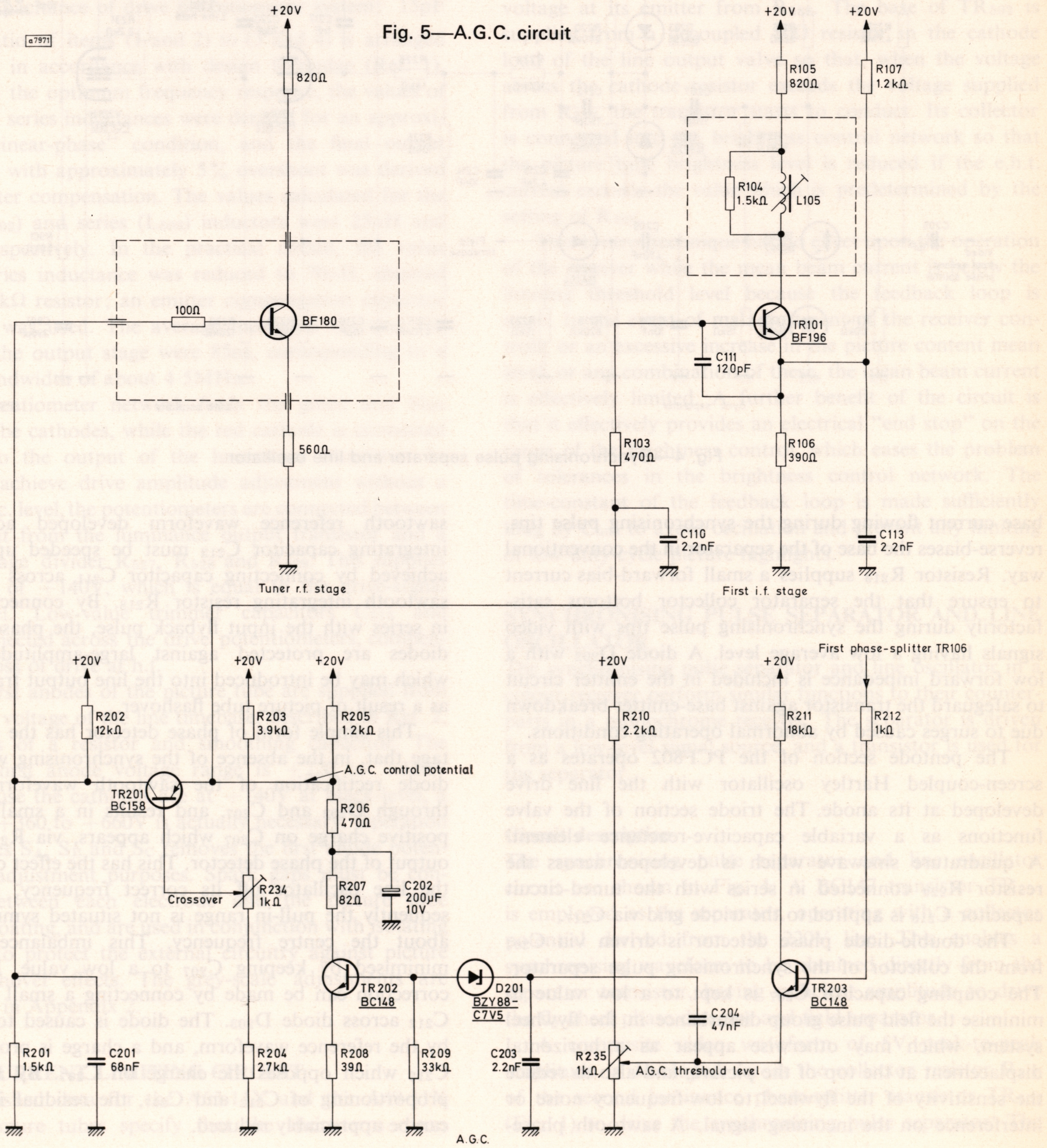
Fig. 5—A.G.C. circuit

Before control, TR$_{203}$ is non-conducting. A current flows through R$_{209}$ and D$_{201}$ into the base of TR$_{202}$, and is sufficient to bottom transistor TR$_{202}$. The a.g.c. potential fed to the a.g.c. control circuit TR$_{201}$ is then defined by R$_{205}$, R$_{206}$, R$_{207}$ and R$_{208}$, and the controlled stages are at maximum gain.

When the synchronising tip level of the input signal exceeds the a.g.c. threshold level setting, TR$_{203}$ conducts pulses of current, the smoothing capacitor C$_{204}$ begins to be discharged and the drop in voltage at the emitter of TR$_{203}$ is fed via D$_{201}$ to the base of TR$_{202}$. The current through TR$_{202}$ therefore falls, and the a.g.c. control potential starts to rise. This increase is fed via R$_{103}$ to the base of the controlled i.f. transistor TR$_{101}$, and its gain begins to be reduced.

Over the range of i.f. control, the control changeover transistor TR$_{201}$ is non-conducting. However, the potential supplied by the network R$_{203}$, R$_{234}$, R$_{204}$ to the base of TR$_{201}$ is set so that, when maximum i.f. control has been attained, TR$_{201}$ starts to conduct. When this happens the potential applied to the base of the controlled i.f. transistor cannot rise further because of the clamping action of the emitter-base diode of TR$_{201}$. However, an increasing current is fed into the emitter of TR$_{201}$ with rising a.g.c. control, and this current flows out of its collector. This raises the voltage across R$_{201}$, and increases the current in the r.f. transistor, thus reducing its gain.

This circuit technique, therefore, permits the control changeover point to be adjusted over a wide range by R$_{234}$, and also ensures that the stopping of i.f. control and the starting of r.f. control are always coincident. Over the range of r.f. control, the variation of control of the i.f. stage is negligible.

COLOUR-DIFFERENCE OUTPUT STAGES

The colour-difference amplifier circuit shown in Fig. 6 uses in the output stages the 40822 package, which comprises three BF179 transistors with turnover voltages selected to suit the requirements of the (R-Y), (G-Y) and (B-Y) output stages. The circuit employs base drive, the output transistors being base driven by normal common-emitter pre-amplifier stages. All stages are partly d.c. coupled to minimise any transient effects, and an overall d.c. feedback system is employed to stabilise the transistor operating conditions. The circuit employs BA145 clamping diodes to ensure constant d.c. conditions at the grids of the picture tube. The circuit is designed to accept the demodulated chrominance signal and is suitable for use with the decoding circuits described in Ref. 4; the circuit provides full drive to the picture tube.

Picture tube requirements

The minimum and maximum peak-to-peak colour-difference drive requirements for an A63-11X colour tube with the cut-off voltage adjusted to 110V (Ref. 5) are:

$E_R'-E_Y'$ drive voltage = 158 to 185V
$E_G'-E_Y'$ drive voltage = 82 to 102V
$E_B'-E_Y'$ drive voltage = 174 to 218V.

This range of drive adjustments can be provided by low wattage preset potentiometers in the collector loads of the output transistors. Fig. 6 shows that the collector load systems for the (R−Y), (G−Y) and (B−Y) output stages are equivalent.

Colour-difference signals are characterised by positive- and negative-going waveforms, and hence the output stages are biased in class A conditions. With the bandwidth required for colour-difference signals, a collector load resistance of 10kΩ is satisfactory with high-frequency compensation. Therefore, the minimum standing collector current in the output stages for full drive across the nominal 10kΩ collector load resistance is given by:

Signal $(E_R'-E_Y')$ = 185V pk−pk

therefore

$$I_c\text{min} = 185/(2\times10^4) = 9{\cdot}25\text{mA}$$

Signal $(E_G'-E_Y')$ = 102V pk−pk

therefore

$$I_c\text{min} = 5{\cdot}1\text{mA}$$

Signal $(E_B'-E_Y')$ = 218V pk−pk

therefore

$$I_c\text{min} = 10{\cdot}9\text{mA}.$$

Collector load networks

In the circuit in Fig. 6 considerable use is made of divided collector loads both in the output stages and the pre-amplifier stages. The use of this system gives important operating advantages:

1) it protects the transistor against the full effect of possible surge voltages after switching on the supply;
2) it prevents the full value of h.t. supply being applied to the collector of the transistor if the stage is momentarily cut off in an overdrive condition;
3) it avoids unnecessary current drain through a transistor when using a relatively low collector voltage compared with the supply voltage and a low value collector resistance.

The calculation of the values in the collector load networks is given in Ref. 5.

Circuit description

In the circuit in Fig. 6, transistors TR$_{506}$ and TR$_{507}$ form the (R−Y) and (B−Y) pre-amplifiers respectively, and base-drive the output stages TR$_{508}$ and TR$_{511}$. The matrixing for supplying the (G−Y) amplifier is carried out in the emitter circuits of the pre-amplifier stages. The resultant (G−Y) signal is then fed to a pre-amplifier TR$_{509}$, which base-drives the (G−Y) output transistor TR$_{510}$.

The output stages have equal gains, hence the gains

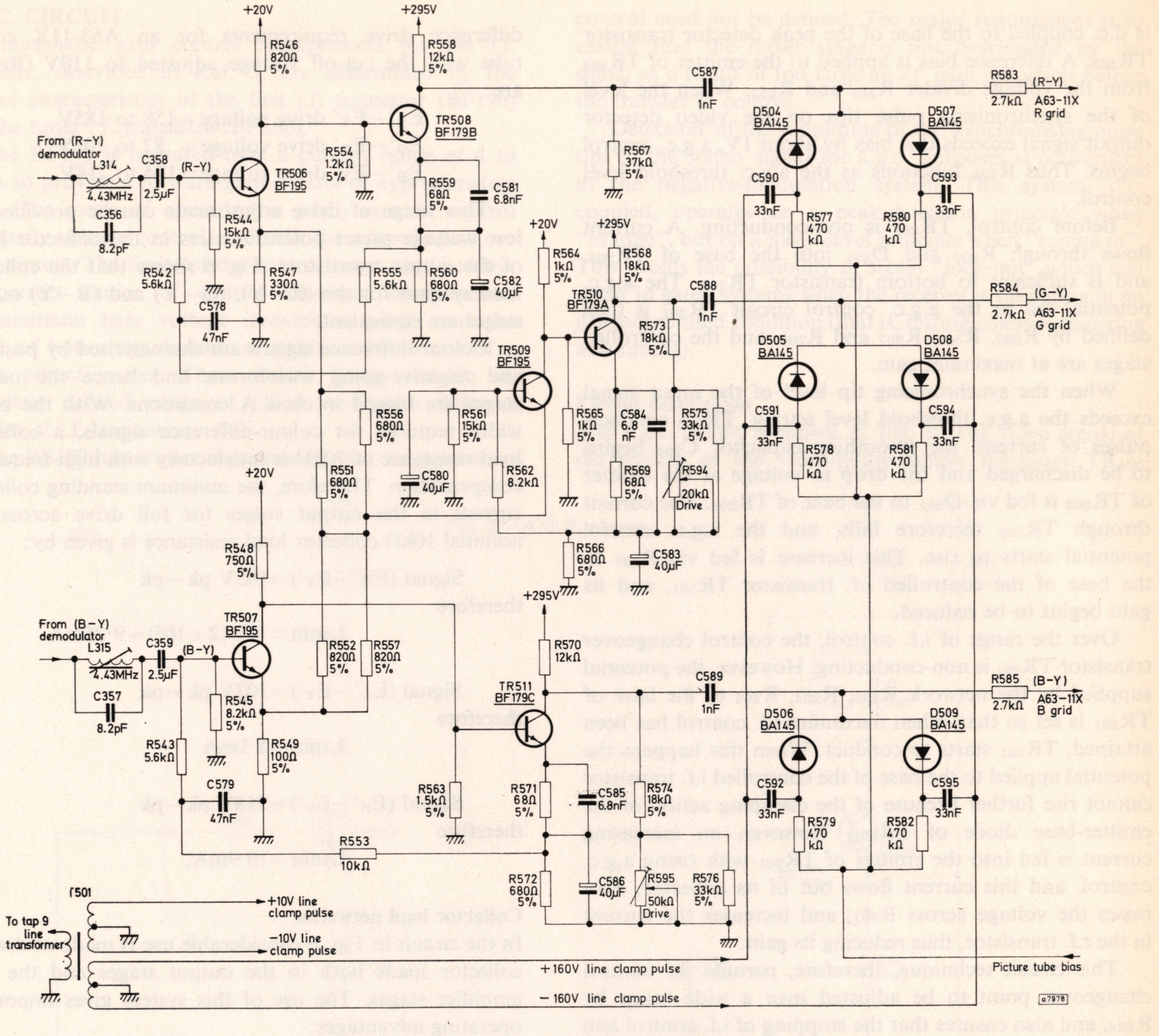
+20V
+295V
R546 820Ω 5%
R558 12kΩ 5%
TR508 BF179B
From (R−Y) demodulator
L314
4.43MHz
C358 2.5µF
(R−Y)
TR506 BF195
R554 1.2kΩ 5%
C356 8.2pF
R544 15kΩ 5%
R559 68Ω 5%
C581 6.8nF
R542 5.6kΩ
R547 330Ω 5%
R555 5.6kΩ
R560 680Ω 5%
C582 40µF
C578 47nF
C587 1nF
R567 37kΩ 5%
R564 1kΩ 5%
R568 18kΩ 5%
TR510 BF179A
TR509 BF195
C588 1nF
R573 18kΩ 5%
R556 680Ω 5%
R561 15kΩ 5%
R565 1kΩ 5%
C584 6.8 nF
R575 33kΩ 5%
R551 680Ω 5%
C580 40µF
R562 8.2kΩ
R569 68Ω 5%
R594 20kΩ Drive
R566 680Ω 5%
C583 40µF
R583 2.7kΩ
(R−Y) A63-11X R grid
D504 BA145
D507 BA145
C590 33nF
C593 33nF
R577 470 kΩ
R580 470 kΩ
R584 2.7kΩ
(G−Y) A63-11X G grid
D505 BA145
D508 BA145
C591 33nF
C594 33nF
R578 470 kΩ
R581 470 kΩ
R548 750Ω 5%
TR507 BF195
From (B−Y) demodulator
L315
4.43MHz
C359 2.5µF
(B−Y)
C357 8.2pF
R545 8.2kΩ 5%
R552 820Ω 5%
R557 820Ω 5%
R543 5.6kΩ
R549 100Ω 5%
C579 47nF
R553 10kΩ
R570 12kΩ
TR511 BF179C
C589 1nF
R571 68Ω 5%
C585 6.8nF
R574 18kΩ 5%
R563 1.5kΩ 5%
R572 680Ω 5%
C586 40µF
R595 50kΩ Drive
R576 33kΩ 5%
R585 2.7kΩ
(B−Y) A63-11X B grid
D506 BA145
D509 BA145
C592 33nF
C595 33nF
R579 470 kΩ
R582 470 kΩ
T501
To tap 9 line transformer
+10V line clamp pulse
−10V line clamp pulse
+160V line clamp pulse
−160V line clamp pulse
Picture tube bias
a7978

Fig. 6—Colour-difference amplifier

of the pre-amplifier stages are proportioned to give the required values of drive to the respective picture tube grids.

A supply voltage of 295V is used for the collector circuit of the BF179 transistors, and 20V for the pre-amplifier stages.

Output stages

In the common-emitter base-drive configuration, the collector-emitter breakdown voltage V_{CEO} is a slightly lower value than V_{CBO}. Therefore, as well as incorporating the divided collector load system, the effective base resistance is made as low as possible together with a low ratio of base resistance to emitter resistance.

An important characteristic of the base drive circuit is that of Miller effect on the coupling network between the pre-amplifier and output stages. This gives a reduction in the gain-bandwidth product of the amplifier as well as the output stage collector circuit. The BF179 has a feedback capacitance C_{re} of about 2·5pF typical, hence with a chosen gain of about 120 times for the output stages, the effective input capacitance of the BF179 will be about 300pF. This will produce a 3dB cut-off frequency point of about 1·1MHz for the 500Ω interstage coupling circuit.

An emitter compensation CR network is used as the main h.f. compensation. This arrangement is useful for h.f. compensation of the interstage circuit as well as the output stage collector circuit.

For a small amount of overshoot in the rise-time characteristic the required value of emitter decoupling capacitor is 6·2nF (Ref. 6). Preferred values of capacitor of either 5·6nF or 6·8nF can be used.

It will be seen that the remaining part of the emitter resistors is bypassed by 40µF electrolytic capacitors. This value ensures that there is negligible droop in the horizontal part of a waveform over a line period. Although this type of emitter circuit produces a partly a.c. coupled stage, the efficient clamp circuits at the picture tube grids prevent any d.c. component errors.

The setting-up procedure for the output stages is given in Appendix 2.

Stage gains in the amplifier

The overall gains for the (R−Y) and (B−Y) channels in the amplifier are 370 and 775 times. With the output stage gains of 120 times, the pre-amplifier gains are, therefore, approximately 3 times and 6·4 times. The effective collector load resistance for the pre-amplifier stages is nominally 500Ω, and the effective emitter resistors for the (R−Y) and (B−Y) pre-amplifier stages will be approximately 165Ω and 78Ω.

Divided collector loads are used for the pre-amplifier stages. The emitter current of the (G−Y) pre-amplifier is also considerably lower than in the (R−Y) and (B−Y) pre-amplifier stages to avoid the undue influence of extra bias on these stages. The collector voltage of these amplifiers is dependent on the biasing condition of the output stage. Also, to relate with preferred values of resistors, the collector currents of the (R−Y), (B−Y) and (G−Y) pre-amplifiers are set at approximately 9mA, 12mA, and 5mA respectively. With an average collector voltage of 7·5V, the following divided load resistor values are obtained:

1) for (R−Y) 820Ω and 1·2kΩ
2) for (B−Y) 750Ω and 1·5kΩ
3) for (G−Y) 1kΩ and 1kΩ.

Matrix system and drive variation

The calculation of the resistor values in the matrix system, and drive variation to the picture tube grids, is given in Ref. 6.

Dissipation in the transistors

The maximum rated dissipation of the BF179 transistor is 1·7W when fitted with a suitable heatsink. The relationship is:

$$P_{c\,max}=(T_j-T_{amb})/R_{th} \qquad (1)$$

where R_{th} is the thermal resistance.

With maximum junction and ambient temperatures of 200°C and 55°C respectively, R_{th} equals 85degC/W. The thermal resistance between the junction and mounting base is given as 40degC/W, hence a heatsink of thermal resistance of not more than 45degC/W should be used for maximum dissipation. Without a heatsink the value of R_{th} is given as 220degC/W, therefore, from Eq.1 the maximum dissipation of the transistor is limited to 660mW. The typical average dissipation figures for the various transistors are given below:

	TR_{506}	TR_{507}	TR_{508}	TR_{509}	TR_{510}	TR_{511}
Dissipation mW	40	70	1525	19·5	725	1630

Clamp circuits

The d.c. restoration is provided by a double-diode clamp circuit as shown in Fig. 6. The circuit, which is of standard form, ensures constant d.c. level at the grids of the picture tube during the blanking period. Equal and opposite clamping pulses of about 160V peak are applied to the 33nF capacitors from a transformer T_{501} fed from tap 9 of the line output transformer (Ref. 2). This level of clamp voltage ensures that the diodes remain in a non-conducting state between pulses for maximum signal drive voltage to the picture tube grid. The transformer T_{501} also provides the ±10V peak line clamp pulses used in the luminance output stage (Fig. 2).

Temperature stability

The variation in collector voltage of each individual stage over the temperature range 20 to 55°C was found to be a very small percentage of the nominal working voltage.

Transformer T_{501} specification

Core: 21mm pot core, type FX2239

All windings are of 42 s.w.g. en. Cu., silk covered.

Primary turns	Secondary turns
40	80+80
	5+5

REFERENCES

1. Fink, D. G. and Hollywood, J. M. **Television Engineering Handbook.** 1st ed. 1957. Video Amplification and D.C. Restoration, Chapter 11, pp. 11.12 to 11.21.
2. Gent, D., Lammers, J., 'Line Timebase and E.H.T. Trebler for Colour Tubes'. **Mullard Technical Communications**, Vol. 10, No. 100, July 1969, pp. 296 to 301.
3. Bissmire, P., 'Single System I.F. Amplifier for U.K. 625-line System'. **Mullard Technical Communications**, Vol. 10, No. 98, March 1969, pp. 234 to 243.
4. Beakhust, D. J., 'Decoding Circuits with Colour-difference Output', to be published shortly in **Mullard Technical Communications.**
5. Hobbs, D. S., 'Hybrid Colour-difference Decoding Circuits'. **Mullard Technical Communications,** Vol. 9, No. 85, Jan. 1967, pp. 111 to 118, and see Vol. 9, No. 86, March 1967, p. 143.
6. Hampson, L., 'Colour Difference Amplifiers using the BF179 Transistor'. **Mullard Technical Communications**, Vol. 9, No. 90, Nov. 1967, pp. 262 to 269.
7. Kallmann, H. E., 'Equalised Delay Lines'. **Proc. I.R.E.,** Vol. 34, September 1946, pp. 646 to 657.

APPENDIX 1

Luminance delay line

Of the various forms of delay line which can be used in the luminance stage of the colour receiver, the type based on the air-cored distributed-element construction has gained considerable favour, because of its low cost and good performance over the required bandwidth. A delay line of this type suitable for a 625-line luminance stage has, therefore, been chosen for the complete receiver design, and descriptions of the design and electrical performance of the line are given here. The design is based on a delay of the order of 600ns.

ELECTRICAL DESIGN

Equalisation

Delay lines with comparatively long delays and composed of distributed elements require equalisation of the higher-frequency delay, otherwise excessive phase distortion occurs. The system used for equalisation in the line described here is based on work by Kallmann (Ref. 7). It consists of a row of copper strips or 'patches' extending the entire length of the delay line. These copper patches are electrically floating and become a form of bridging capacitances, which compensate for the effective loss of inductance in the line at the higher frequencies. By careful adjustment of the size of the patches, delay equalisation within 1 to 2% can be achieved over a wide frequency range.

Characteristic impedance

The delay per unit length of delay line decreases as the impedance of the line increases. The impedance is a compromise between such factors as the ease of termination, drive requirements and physical size. A value of 1kΩ has been chosen here as a good compromise between drive requirements and external termination effects. When a driver transistor is used at the input to the line, a signal power of about 10mW is required at the collector to produce subsequent full drive for the picture tube, yet (as shown in Fig. 7) only a very minor change is made in the delay line performance when the end of the line is shunted with a 33pF capacitor to represent the input of the following video stage. In addition, a 1kΩ delay line can be reasonably short (approximately 105mm) and it can have a small insertion loss.

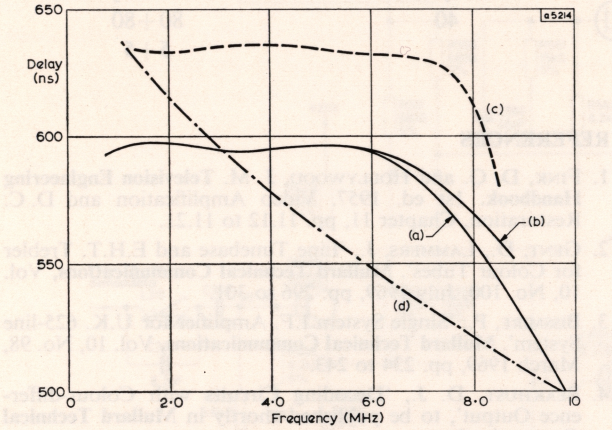

Fig. 7—Delay characteristics for:
(a) Delay line containing 10 patches, 9×3mm
(b) Delay line (a) with 33pF capacitor at end of line
(c) Delay line containing 12 patches, 8×3·5mm
(d) Unequalised delay line

PHYSICAL CONSTRUCTION

The component parts of the prototype line are shown in Fig. 8. To form the distributed shunt capacitance, three earthed copper strips, two each of 5mm width and one of 4mm width, are placed around the body of the length of Tufnol rod, with a gap of about 0·5mm between adjacent strips. In this form, a gap of approximately 5mm is left between adjacent sides of the two outer strips.

The dielectric foils consists of a 45mm width of Melinex polyester sheet of 0·001 inch thickness. Fig. 8 shows the sheet containing the length of copper foil compensating patches. The width of the sheet allows two layers to be wound on the former and the final layer brings the copper patches to lie in the 5mm gap between the copper strips.

The former length allows a nominal 1350 turns of 46 s.w.g. self-fluxing enamelled wire to be wound uniformly over the dielectric foil. Lead-through pins provide suitable terminal points at each end of the former. In quantity a printed plastic film would simplify fabrication and give very consistent results.

ELECTRICAL PERFORMANCE

In Fig. 7 the variations of delay with frequency are shown for two sample sets of patches. Curves (a) and (b) were determined with a line containing a row of ten patches, 9·0×3·0mm and curve (c) shows the performance of a line with twelve patches, 8·0×3·5mm. The figures show how the lines can be equalised by these single rows of patches to within 2% up to about 6 to 7MHz. Curve (d) shows the typical performance of an uncompensated line and indicates the excessive phase distortion without compensation.

Applying a step waveform of moderate rise time (not greater than 20ns) at the input of the lines produces a smoothly rising output waveform, substantially free from pre-shoot or overshoot. The measured rise time of both samples was about 120ns.

The two examples are intended to show that it is useful to experiment with small variations in the number and size of patches along the line before a final choice is made, because of the empirical nature in the fine adjustment of the delay equalisation. Once the number and size of patches along the line are decided, repeatable results can be achieved simply. The small changes in the patches, as described above, do not produce any substantial change in the characteristic impedance of the line. Fig. 9 shows an average curve of insertion loss plotted against frequency. When measured with a square-wave input voltage, the indicated insertion loss was of the order of 1·5dB.

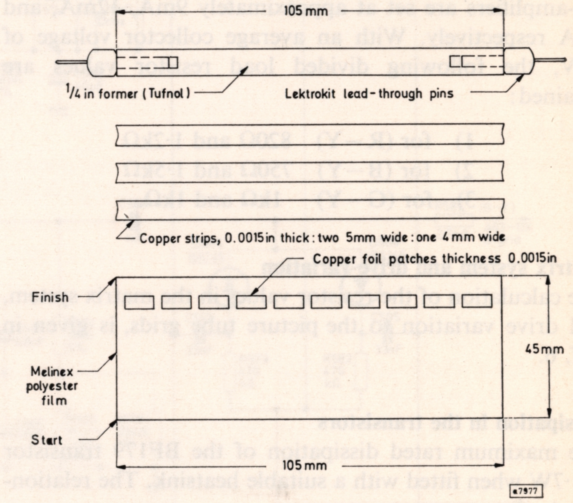
105 mm
1/4 in former (Tufnol)
Lektrokit lead-through pins
Copper strips, 0.0015in thick: two 5mm wide: one 4mm wide
Copper foil patches thickness 0.0015in
Finish
Melinex polyester film
Start
45mm
105 mm
a7977

Fig. 8—Constructional details of delay line

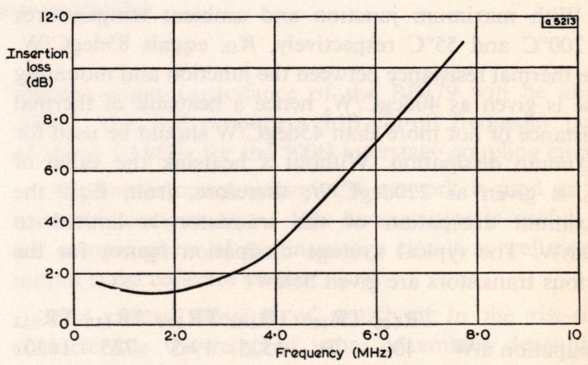

Fig. 9—Insertion loss

The electrical performance of the experimental lines is summarised as follows:

Nominal characteristic impedance	1 kΩ
Nominal delay	600 ns
Rise time	120 ns
Average insertion loss	1·5dB
Equalisation	Within 2% up to 7 MHz

APPENDIX 2

Grey-scale and colour-difference adjustments

GREY-SCALE ADJUSTMENTS

To obtain good grey-scale operation, it is necessary to adjust the drive conditions of the three electron guns carefully for each individual picture tube. Grey-scale tracking is obtained by initially setting the cut-off voltage of each electron gun to the same value, and then adjusting the luminance drive to obtain the correct white point. A grid cut-off voltage of −120V is chosen so that the rated beam current can always be obtained. Since the picture tube cathodes are directly coupled to the luminance stage, their black-level voltage (cut-off) point is fixed at +140V. Therefore, the grid clamps are returned to +30V giving a −110V setting for cut-off.

Adjustment is carried out by setting the anode voltage of the luminance output stage at +140V on a blank raster by means of the brightness control, and then varying the first anode potentials by means of the three preset potentiometers, R_{591}, R_{592}, R_{593} in Fig. 2. Switches S_A, S_B and S_C for the three guns facilitate the separate adjustment of the three potentials.

The cut-off values having been set, the drives applied to the blue and green guns are adjusted for a good peak white colour on a test step-wedge pattern. A further slight adjustment may be made, if necessary, to improve the colour neutrality in the dark grey region. This must be followed by a final adjustment of the luminance drives for white.

For a correct grey-scale with cathode drive, taking into account picture spreads, the range of full drive voltages required when the cut-off voltages are set to −110V are:

Red cathode	100 to 87V
Blue cathode	94 to 74V
Green cathode	96 to 76V

COLOUR-DIFFERENCE DRIVE ADJUSTMENT

These adjustments are best carried out by reference to a colour-bar signal displayed on the picture tube. Initially, the contrast control is set to about 80% maximum; then with the blue and green guns switched off, the chrominance preset saturation control is adjusted until the two pairs of red bars are of equal brightness. Having achieved this relative setting of contrast and chrominance saturation, the blue colour-difference drive is adjusted with the red and green guns turned off so that bars of equal brightness are obtained.

Finally, the green drive is adjusted to cancel the luminance gradation on the bright and dark halves of the green gun picture. These comparatively subjective adjustments using the visual output of the picture tube give quite consistent results and require very short setting-up times.

Transistor Audio and Radio Circuits

The Mullard book "Transistor Audio and Radio Circuits" is intended as a manual of established and practical circuits for use by receiver and equipment manufacturers, radio and audio service engineers, university and college students, and do-it-yourself home constructors and hi-fi enthusiasts. A wide range of circuits is presented, extending from complete portable radio receivers to f.m. tuners and audio amplifiers capable of the highest standards of reception and reproduction. The audio amplifiers included in the book are listed below.

A. F. Amplifier Circuits

Output power (W, r.m.s.)	Total harmonic distortion (%)	Sensitivity (mV input for full output)	Recommended use
1	10	10	general purpose
3	1·7	70	general purpose
3	0·4 to 2	600	record player
4	1·2	0·4	tape recorder
5	2·5	43	car radio
6	1·2	52	car radio
10	2·9	80	general purpose
10	<0·1	430	high-quality systems
25	0·2	200	high-quality systems

Subjects include:

Pre-amplifiers for use with most a.f. circuits; r.f. circuits for a.m. and a.m./f.m. portable radios and car radios; auxiliary high-quality a.f. and r.f. "building block" circuits; high-quality f.m. tuners and stereo decoder; test equipment; hints on layout of high-quality a.f. equipment; biasing of r.f. circuits; useful charts and nomograms.

The book may be obtained from booksellers or Distributor Sales Division, Mullard Limited, Mullard House, Torrington Place, London, W.C.1., price (U.K. only) 30/- plus 2/- postage.

Thermostatic fan control for central heating

S. W. Gray
Mullard Central Application Laboratory

UDC 697.3:621.61/63:621-523:536.58[621.382]

This article describes an electronic circuit that varies the speed of a fan inversely proportional to temperature over a limited band of temperature. For temperatures above the proportional band the circuit turns the fan off and for temperatures below it full current is supplied to the fan.

The application of the circuit is principally to central heating appliances.

INTRODUCTION

Fans are employed in many central heating appliances, such as warm air systems, fan convector radiators, off-peak electric fan storage radiators, and electric fan heaters. All of these heating systems may be thermostatically controlled, but only those whose heat output is proportional to fan speed can be controlled by means of fan speed alone: this fact restricts this system of control to fan convector radiators, off-peak electric fan storage radiators, and Electricair systems because other heat sources supply constant heat regardless of air velocity.

Modulation of heat output is desirable with all forms of heating, but with warm air systems it becomes very important since discomfort is often experienced with on-off types of control because of the sudden small changes in temperature and ventilation rate inherent with this form of control.

The electric fan control circuit described in this article is capable of modulating a hot air supply to give just the correct amount of heat to provide a comfortable temperature over a wide range of conditions without overshoot.

REQUIREMENTS FOR MODULATING FAN CONTROLLER

If simple proportional control only is used, a long time may elapse before the desired temperature is reached. Hence full output is required at temperatures just below the desired level and zero output just above. In between, proportional control is desirable, the actual mean level being adjustable to suit individual needs: the fan output is made inversely proportional to temperature in this range for heating applications. If the proportional control range is too narrow, the control will tend to behave as an on-off control, and so a compromise is necessary. In practice a proportional temperature range of about 2degC gives a satisfactory performance.

CIRCUIT DESCRIPTION

A full wave bridge rectifier in addition to a thyristor (Fig. 1) provides full wave a.c. power control essential for the induction fan motor. In this circuit the bridge rectifier D_3 to D_6 is also used to supply current to the trigger circuit and temperature sensor.

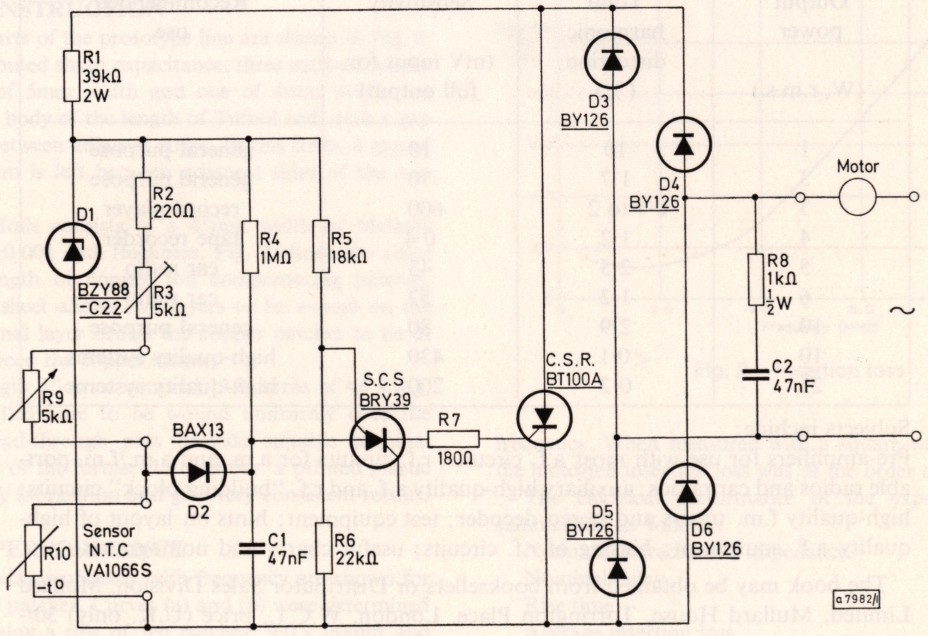

Fig. 1.—Fan control circuit

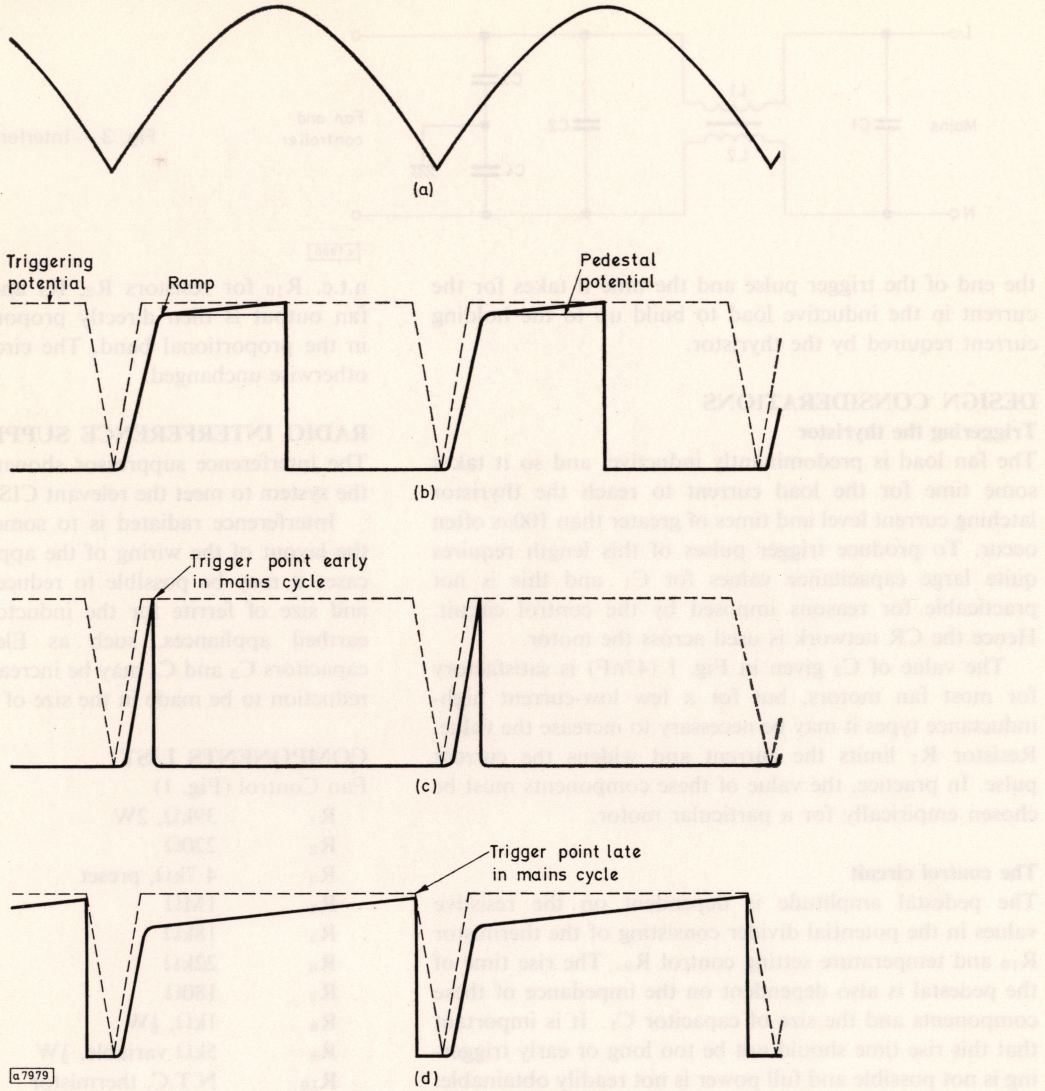
(a)
Triggering potential
Ramp
Pedestal potential
(b)
Trigger point early in mains cycle
(c)
Trigger point late in mains cycle
(d)
a7979

Fig. 2.—Triggering capacitor waveforms
(a) rectified mains waveform for reference
(b) temperature at (or near) 'set temperature'
(c) temperature much lower than 'set temperature'
(d) temperature much higher than 'set temperature,

The trigger circuit is of the so called 'ramp and pedestal' type in which the triggering capacitor C_1 is charged rapidly via D_2 to a level determined by potential divider R_2, R_3, R_9, and the n.t.c. resistor, R_{10}. It then continues to be charged at a much slower rate through resistor R_4 either until it reaches the s.c.s. triggering potential (which is determined by potential divider R_5 and R_6, together with the anode-anode gate voltage of the s.c.s.) or until the end of the mains cycle occurs. It can be seen (Fig. 2b) that, for pedestal voltages just below the triggering level, the s.c.s. will trigger at some point along the ramp, and a variation in pedestal amplitude about this value will result in a proportional variation of the triggering angle.

The pedestal amplitude is determined by a combination of the temperature, via the n.t.c. resistor, and the 'set temperature' control R_9, so for a given 'set temperature' the triggering angle is proportional to temperature. For wide downward temperature excursions from the 'set temperature' level the pedestal amplitude will be higher than the trigger potential, providing a small fixed triggering angle which results in nearly full power being supplied to the fan (Fig. 2c). With wide upward temperature excursions the reverse action occurs and hence very little power is applied to the motor (Fig. 2d). The pre-set resistor R_3 allows the set temperature control to be centred, allowing for component spreads.

The potential of the trigger circuit is stabilised by the voltage regulator diode D_1 supplied from the full wave bridge, D_3 to D_6. This arrangement ensures a consistent trigger pulse over all normal triggering angles and the performance is independent of mains voltage variations. The resistor R_7 is provided to give the optimum length trigger pulse from C_1 and to limit the peak current through the s.c.s. The CR network consisting of C_2 and R_8 is necessary to provide the thyristor latching current between

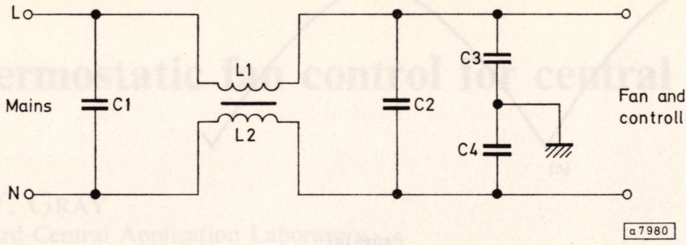

Fig. 3.—Interference suppressor

the end of the trigger pulse and the time it takes for the current in the inductive load to build up to the holding current required by the thyristor.

DESIGN CONSIDERATIONS

Triggering the thyristor

The fan load is predominantly inductive, and so it takes some time for the load current to reach the thyristor latching current level and times of greater than 100µs often occur. To produce trigger pulses of this length requires quite large capacitance values for C_1 and this is not practicable for reasons imposed by the control circuit. Hence the CR network is used across the motor.

The value of C_2 given in Fig. 1 (47nF) is satisfactory for most fan motors, but for a few low-current high-inductance types it may be necessary to increase the value. Resistor R_7 limits the current and widens the current pulse. In practice, the value of these components must be chosen empirically for a particular motor.

The control circuit

The pedestal amplitude is dependent on the resistive values in the potential divider consisting of the thermistor R_{10} and temperature setting control R_9. The rise time of the pedestal is also dependent on the impedance of these components and the size of capacitor C_1. It is important that this rise time should not be too long or early triggering is not possible and full power is not readily obtainable. A rise time of about 12ms is a good design value. Values less than this necessitate the use of a lower resistance thermistor; this gives self heating problems and, furthermore, at these early triggering angles the anode voltage of the thyristor is low enough to give additional problems with latching and holding current. Longer values of rise time result in an appreciable drop in the maximum motor power.

The ramp amplitude is controlled simply by resistor R_4 and this determines the width of the proportional band of temperature. The value given in Fig. 1 (1MΩ) should be satisfactory for most applications but where wider or narrower proportional bands are needed a change of value of R_4 is all that is required.

USE OF SYSTEM FOR COOLING

For cooling purposes the fan can easily be made to operate only above the set temperature by changing the n.t.c. R_{10} for resistors R_2, R_3 and R_9, and vice versa: fan output is then directly proportional to temperature in the proportional band. The circuit operation remains otherwise unchanged.

RADIO INTERFERENCE SUPPRESSION

The interference suppressor shown in Fig. 3 will enable the system to meet the relevant CISPR and BS limits.

Interference radiated is to some extent dependent on the layout of the wiring of the appliance so that in some cases it may be possible to reduce the number of turns and size of ferrite for the inductors. With permanently earthed appliances, such as Electricair systems, the capacitors C_3 and C_4 may be increased, enabling a further reduction to be made in the size of the inductors.

COMPONENTS LIST

Fan Control (Fig. 1)

R_1	39kΩ, 2W	
R_2	220Ω	CR25/220
R_3	4·7kΩ, preset	E097AD/4K7
R_4	1MΩ	CR25/1M
R_5	18kΩ	CR25/18K
R_6	22kΩ	CR25/22K
R_7	180Ω	CR25/180
R_8	1kΩ, ½W	
R_9	5kΩ variable, ½W	
R_{10}	N.T.C. thermistor	VA1066S
C_1	47nF	C280AE/P47K
C_2	47nF	C280CF/P47K
D_1	Voltage regulator diode	BZY88–C22
D_2	Diode	BAX13
D_3 to D_6	Rectifier diodes	BY126
S.C.S.	Silicon controlled switch	BRY39
C.S.R.	Thyristor	BT100A

Interference Suppressor (Fig. 3)

C_1	100nF
C_2	100nF
C_3	4·7nF
C_4	4·7nF
L_1 and L_2	250 turns each on separate bobbins. Both bobbins on 12mm Mullard A4 ferrite rod